

# Plano Intel 11.6" Schematics Document

## Baytrail M

**2014-12-29**  
**REV : A00**

*DY : None Installed*  
*XDP: For CPU XDP Debug Port installed*

<Core Design>



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Title

**Cover Page**

Size  
A3

Document Number

**Plano 11.6" BTM**

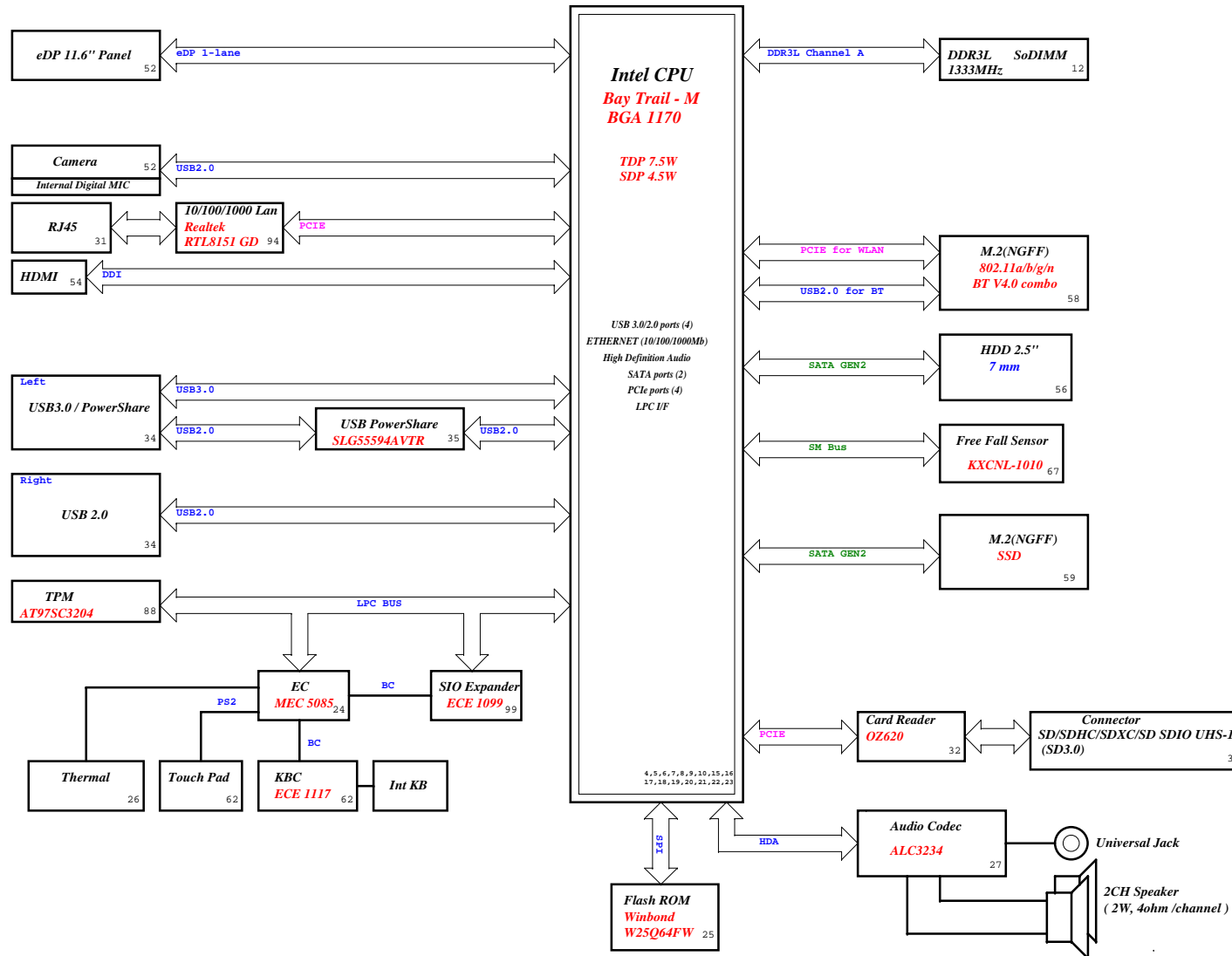
Rev  
**A00**

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# Plano 11.6" Block Diagram

Project code : 4PD021010001  
PCB P/N : 14230  
Revision : -1



CHARGER	
BQ24715	44
INPUTS	OUTPUTS
AD+ BT+	DCRATOUT
SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
DCRATOUT	3D3V_AUX_S5 3D3V_S5 5V_S5
CPU DC/DC	
ISL95833	46-48
INPUTS	OUTPUTS
DCRATOUT	VCC_CORE GFX_CORE
SYSTEM DC/DC	
SY8206DQNC & RT8068A	50
INPUTS	OUTPUTS
DCRATOUT	ID0V_S5 ID0V_S0
SYSTEM DC/DC	
SY8206DQNC & APL5338	49
INPUTS	OUTPUTS
DCRATOUT	ID33V_S3 ID067V_S0 ID06_VREF_S3
SYSTEM DC/DC	
S-1339D15-M5001 S-1339D18-M5T1U3	51
INPUTS	OUTPUTS
3D3V_S5	ID5V_S0 ID8V_S0
Load Switches	
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0 3D3V_LAN LCDVDD ID33V_S5 ID8V_S5 ID0V_S5
PCB LAYER(FR4-6 Layer)	
L1:Top L2:PWR/GND L3:Signal L4:Signal L5:PWR/GND L6:Bottom	

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<b>Block Diagram</b>			
Size A2	Document Number	<b>Plano 11.6" BTM</b>	Rev <b>A00</b>
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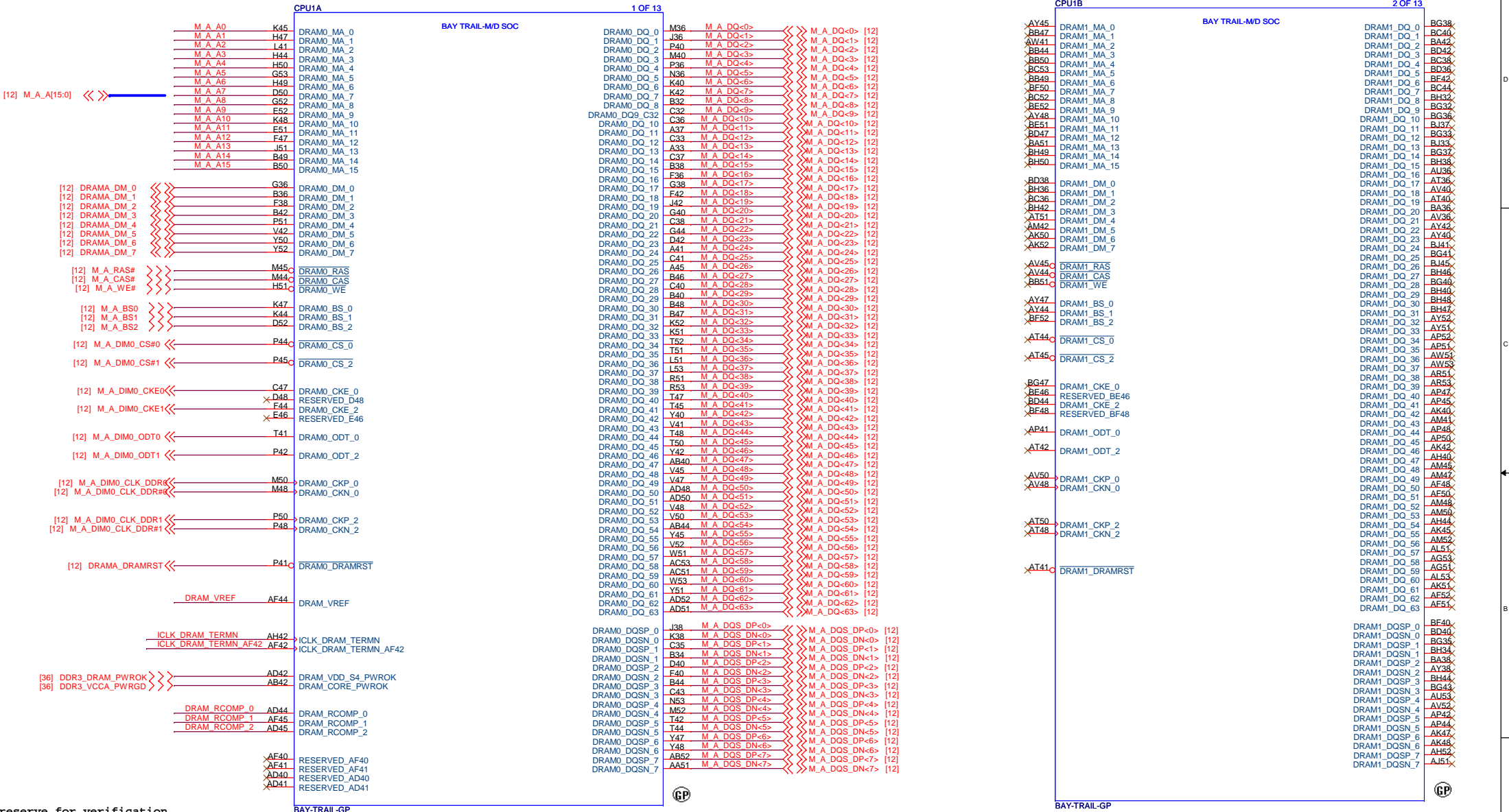
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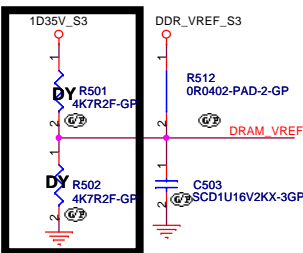
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SSID = CPU



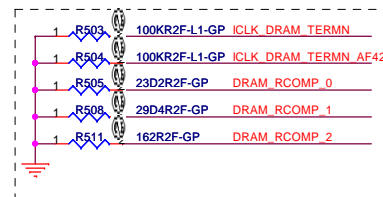
reserve for verification



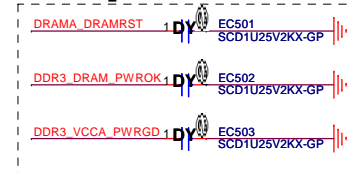
PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M\_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

NOTE:  
PLACE 0.1U CAP CLOSE TO CPU

Note: All RCOMP resistors have ±1% tolerance



EMI caps.



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**CPU (DDR)**

Plano 11.6" BTM


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SSID = CPU

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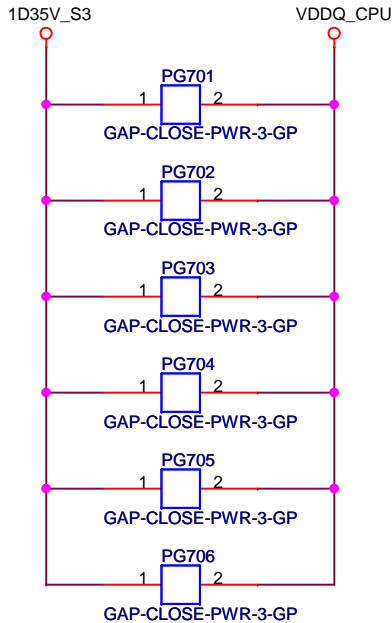


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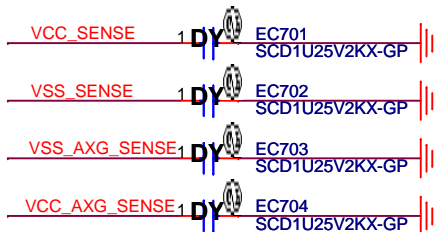
Title		
CPU (CFG)		
Size	Document Number	Rev
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SSID = CPU

VDDQ\_CPU



EMI Caps.



Parallel

[47] VCC\_SENSE <<<  
[47] VSS\_SENSE <<<

Parallel

[48] VSS\_AXG\_SENSE <<<  
[48] VCC\_AXG\_SENSE <<<

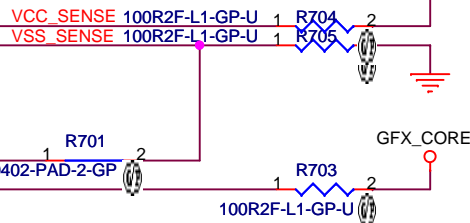
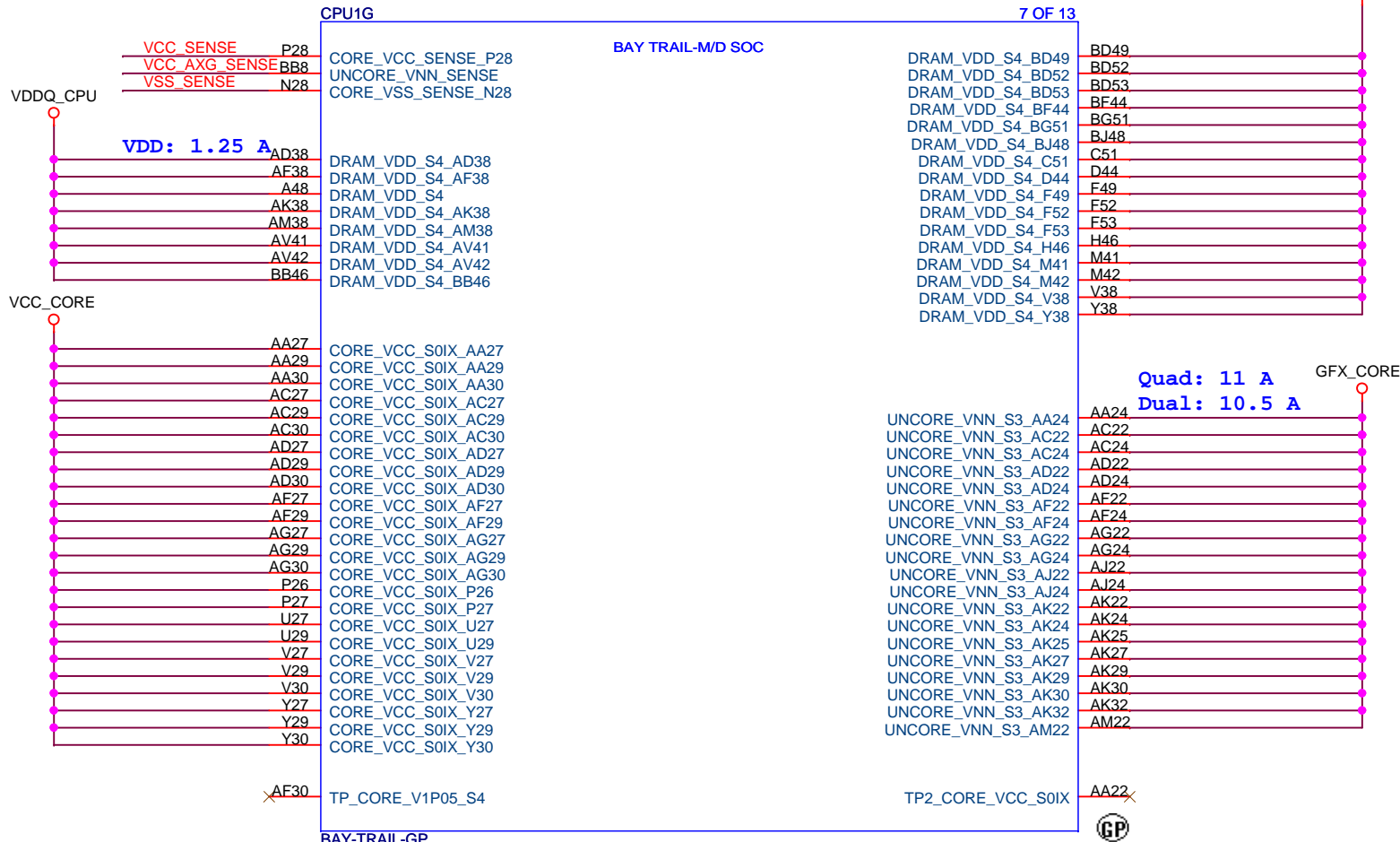


Table 53. VCC and VNN Currents

SKU	VCC Icc Max	VNN Icc Max
N3520 - Quad Core Pentium	10.5 A	10.5 A
N2920 - Quad Core Celeron	8.5 A	10.5 A
N2820 - Dual Core Celeron	5.2 A	10.5 A
N2815 - Dual Core Celeron	5.2 A	10.5 A
N2806 - Dual Core	4 A	7 A
J2900 - Quad Core Pentium	13.5 A	11 A
J1900 - Quad Core Celeron	10.5 A	11 A
J1800 - Dual Core Celeron	7 A	10.5 A



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**CPU (VCC CORE)**

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A4

Document Number

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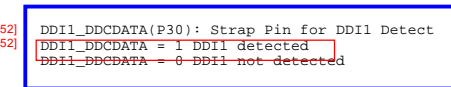
Rev

**A00**

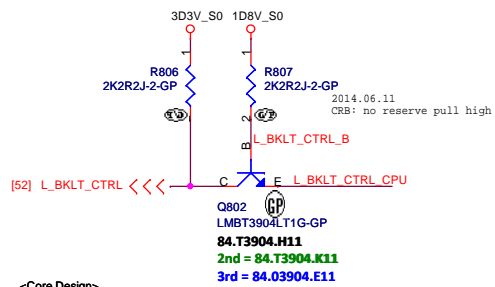
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```
DDIO0_DDCDATA(C26): Strap Pin for DDIO0 Detect
DDIO0_DDCDATA = 1 DDIO0 detected
DDIO0_DDCDATA = 0 DDIO0 not detected
```

[illegible]

## Level shift



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CPU (DDI/EDP/GPIO)

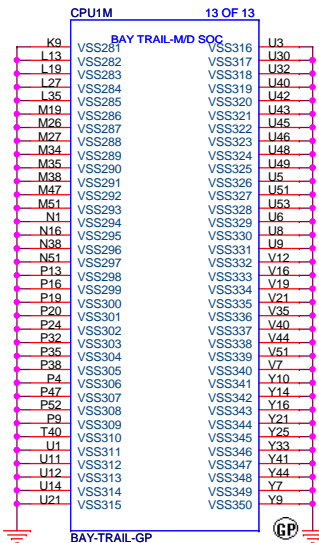
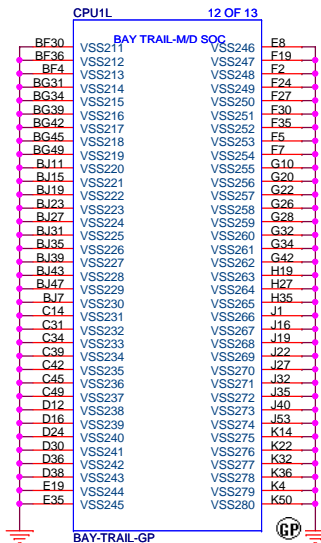
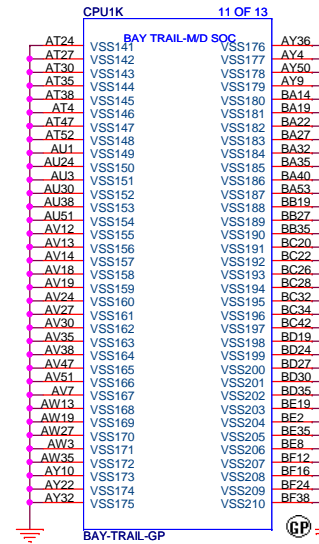
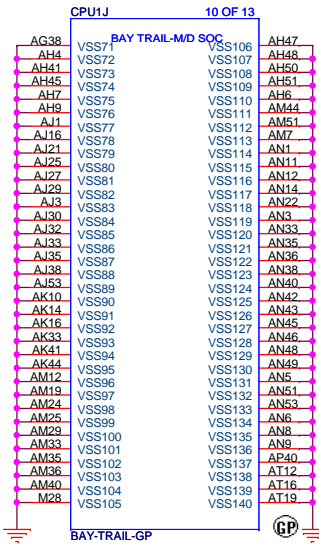
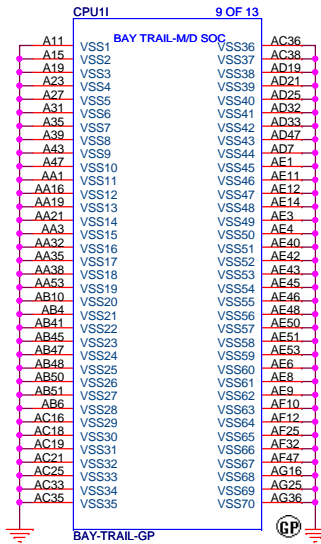
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SSID = CPU



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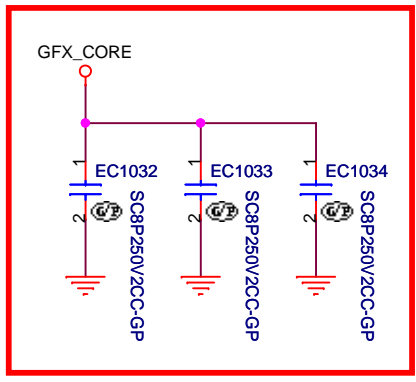
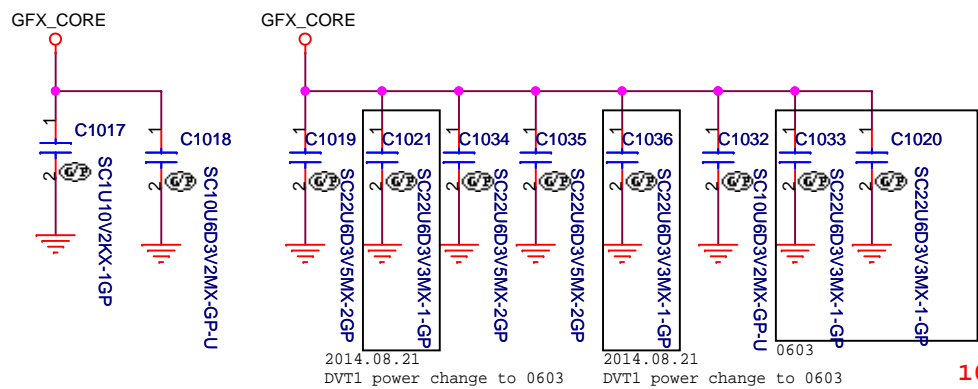
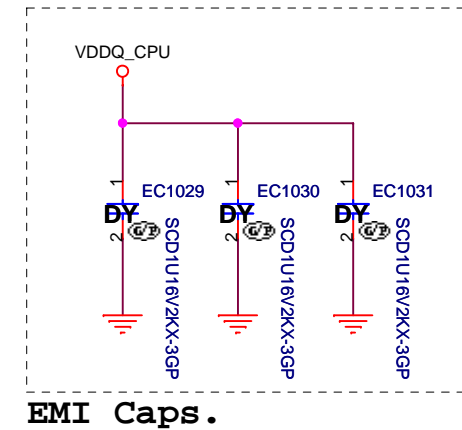
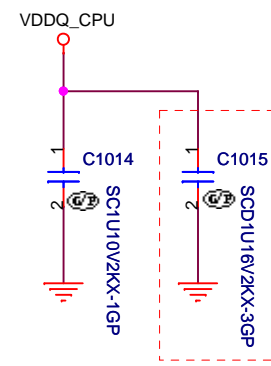
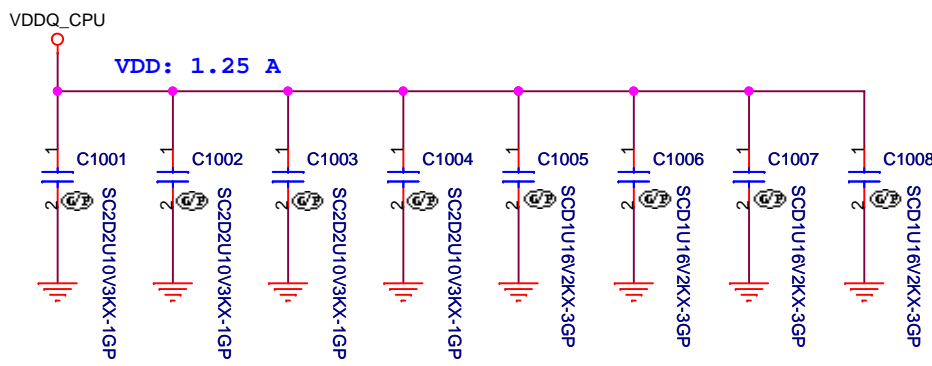
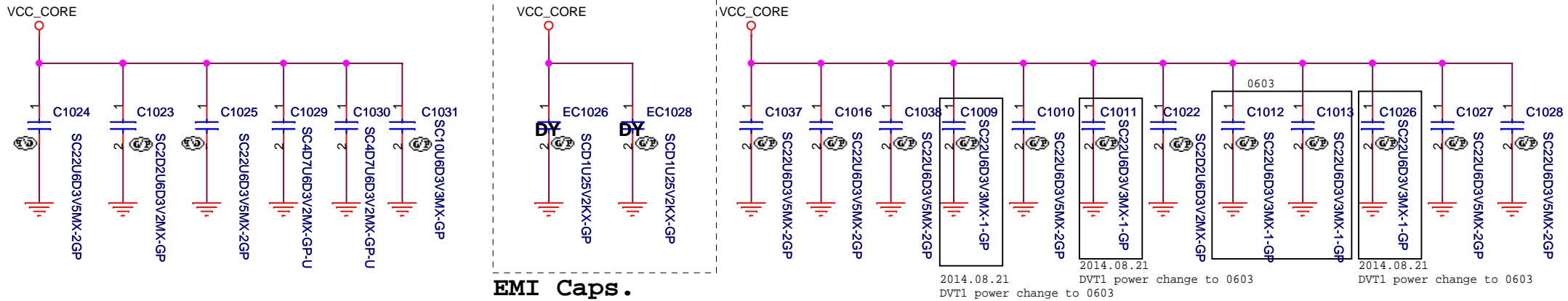
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Title: **CPU (VSS)**

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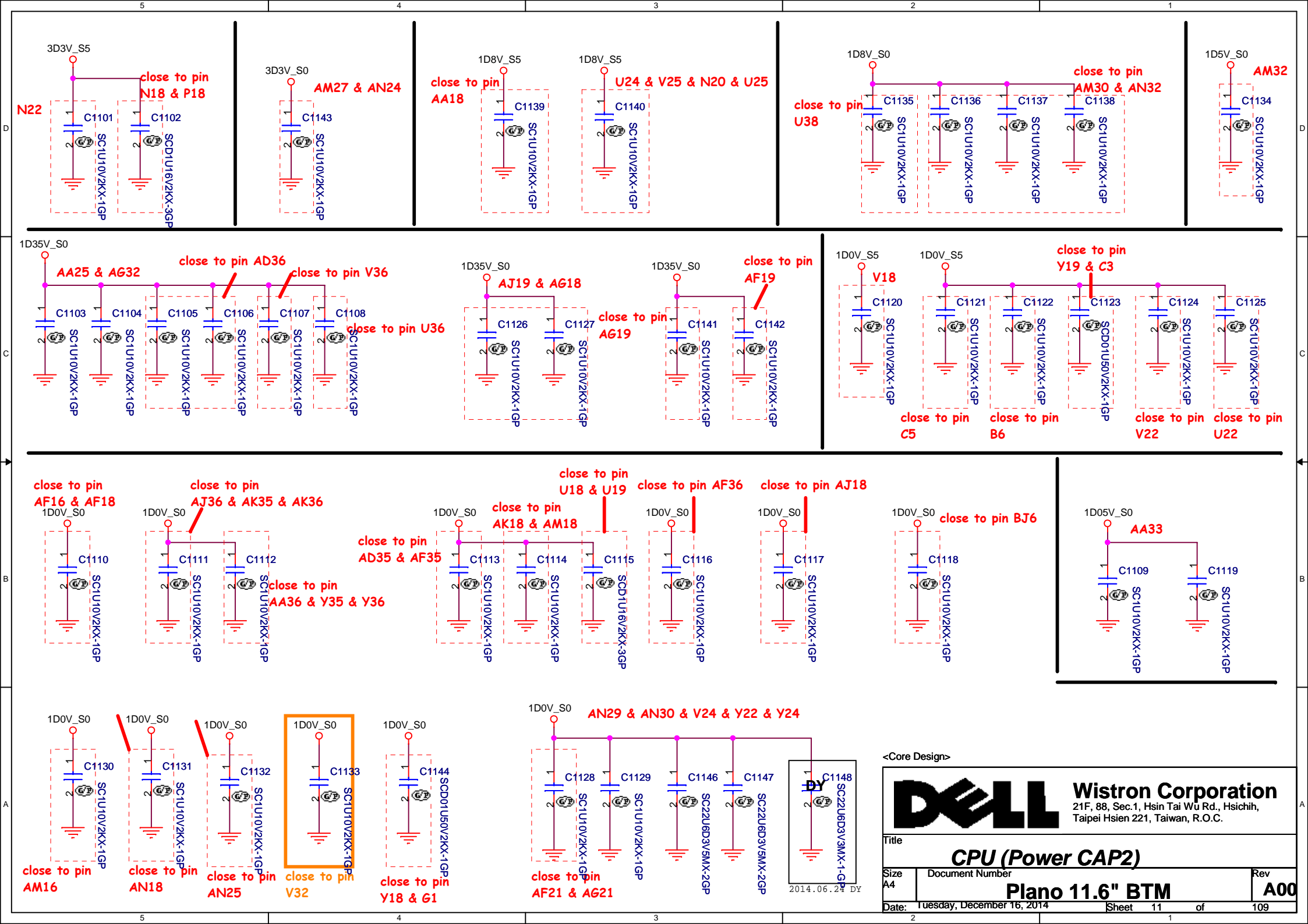
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Title  
**CPU (Power CAP1)**

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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

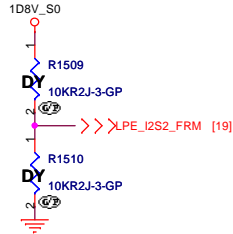
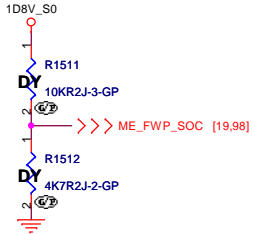
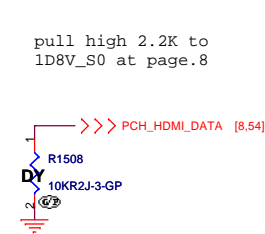
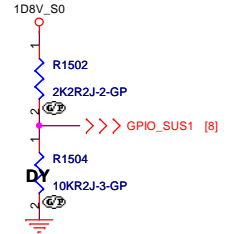
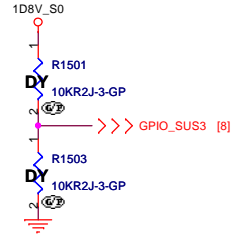
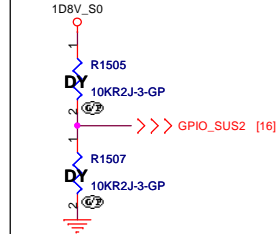
Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap (A16 Override)
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [056]
Schematic						
High	SPI (Default) Internal PH	Normal Operation (Default) Internal PH	DDI0 detected	DDI1 detected	DDI1 detected	Top address bit is unchanged (Default) Internal PH
Low	LPC	Override	DDI0 not detected (Default)	DDI1 not detected (Default)	DDI1 not detected	Top address bit is inverted

Table 20. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is inverted 1 = Top address bit is unchanged
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

#### 27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

**Note:** The Top-Swap strap is an active high signal and is multiplexed with the GPIO\_S0\_SC[56] signal.

Signal Name	Dir	Term	Plat. Power
GPIO_S0_SC[056]†	I/O	20k,H	V1P8S
GPIO_S0_SC[063]†	I/O	20k,H	V1P8S
GPIO_S0_SC[065]†	I/O	20k,H	V1P8S

#### 30.2 LPE\_I2S2\_DATAOUT/ GPIO\_S0\_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO\_S0\_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

Signal Name	Dir	Term	Plat. Power
DDI0_DDCDATA†	I/O	20k(L)	V1P8S
DDI1_DDCDATA†	I/O	20k(L)	V1P8S

INTEL BTM EDS Rev2.5

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Title			CPU(STRAP)	
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SSID = PCH

Close to CPU

Avoid routing next to clock/high speed signals.

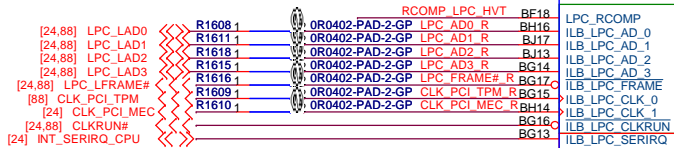
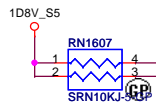
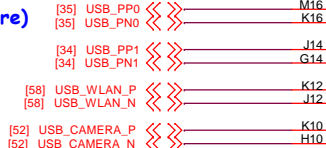
Connected to package ground.

USB 3.0(power share)

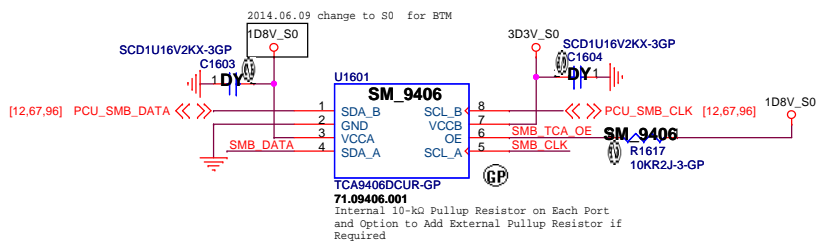
USB 2.0

WLAN

Camera



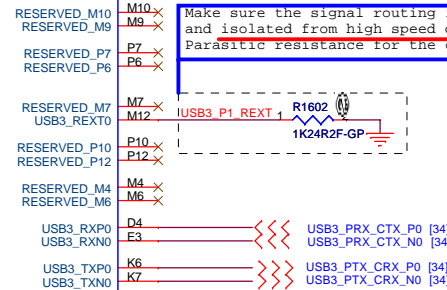
PCU_SMB_ALERT#	I (OD) TBD	SMBus Alert
		This signal is used by SMBus devices to wake the system or generate SM#*. This signal is open drain, and it has 20 kΩ internal pull-up. This signal is muxed and may be used as a GPIO.



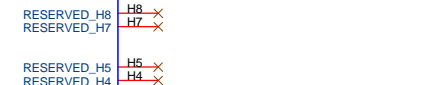
CPU1F

BAY TRAIL-M/D SOC

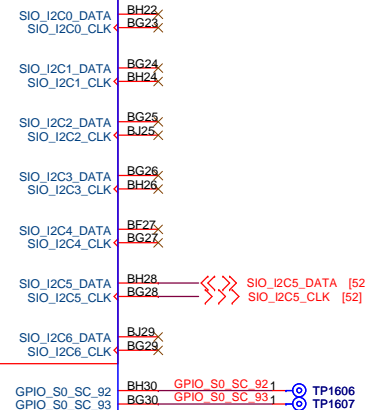
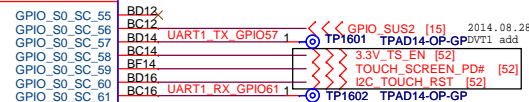
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Make sure the signal routing is as short as possible and isolated from high speed data signal.  
Parasitic resistance for the overall routing should be less than 100 Ω.



GPIO\_S0\_SC [56](BC12): Top swap (A16 Override)  
GPIO\_S0\_SC\_56 = 1 Top address bit is unchanged (Default)  
GPIO\_S0\_SC\_56 = 0 Top address bit is inverted



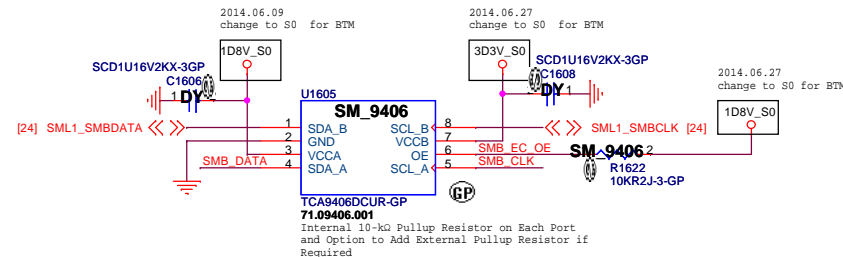
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VLPC:3.3 V

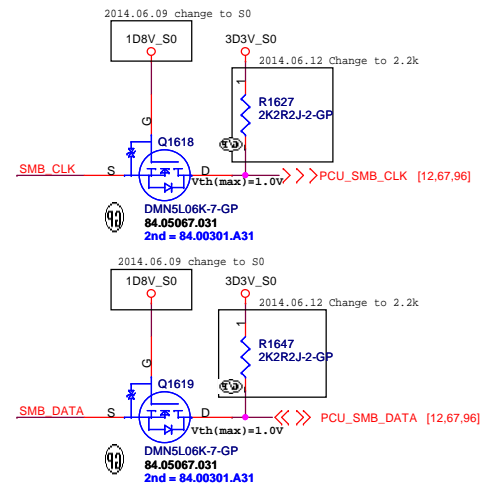
V1P8S

1.8V

BAY-TRAIL-GP



Level shift



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File: CPU (USB/LPC/GPIO)  
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Title

***CPU (Reserved)***

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A4

Document Number

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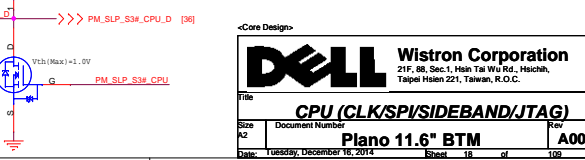
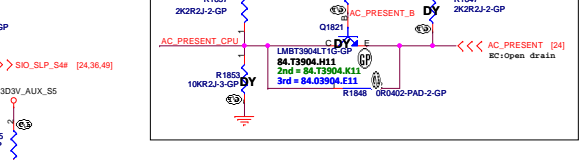
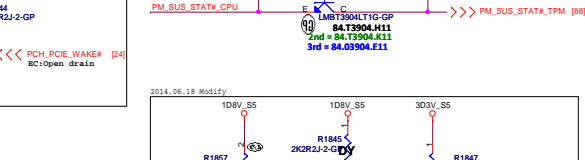
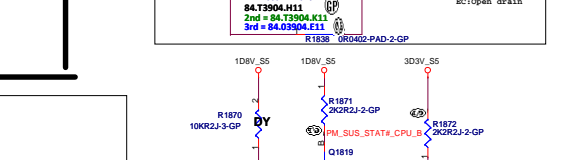
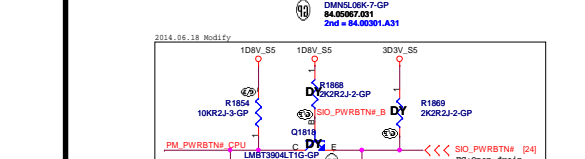
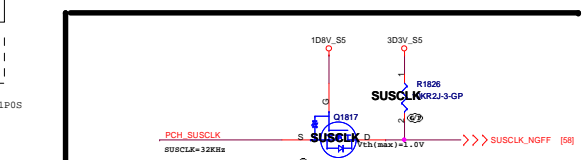
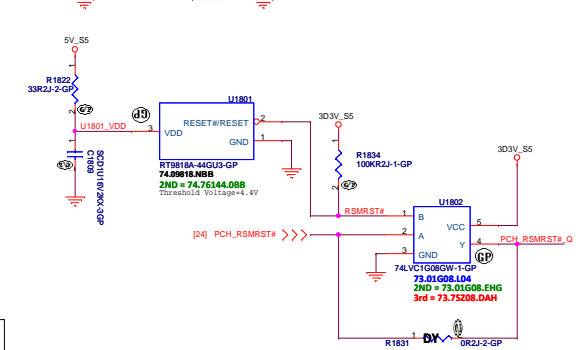
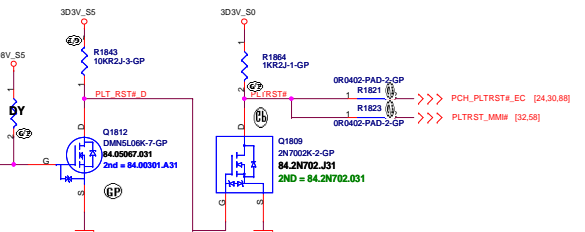
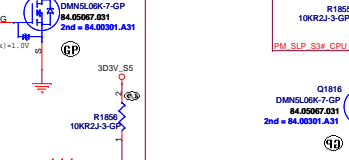
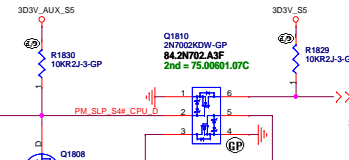
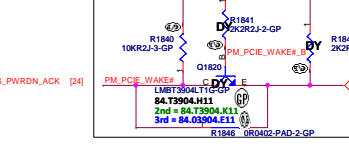
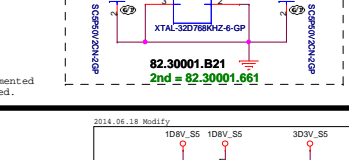
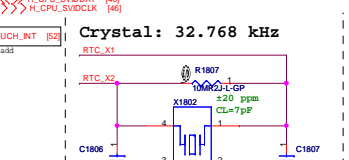
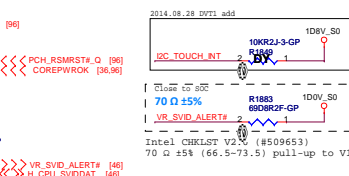
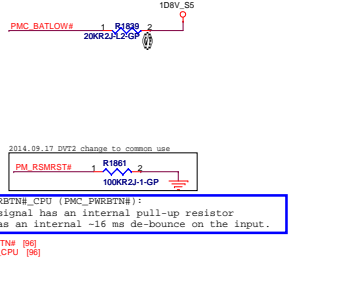
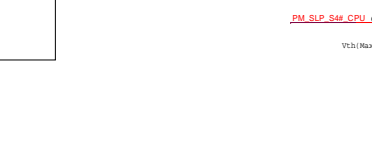
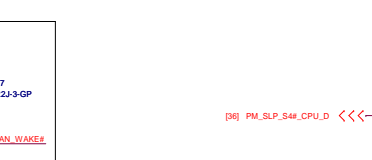
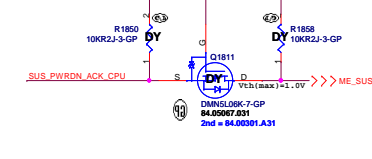
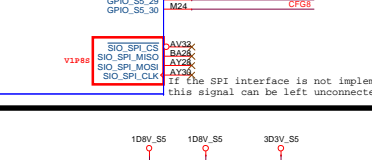
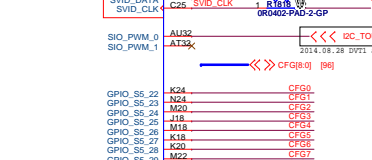
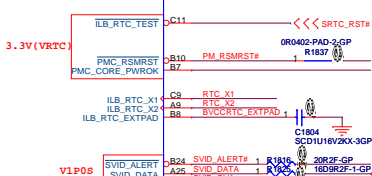
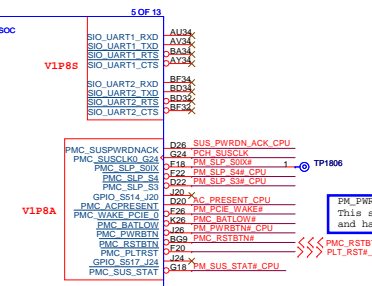
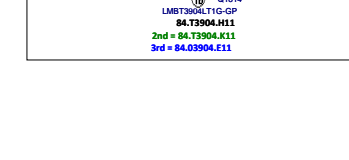
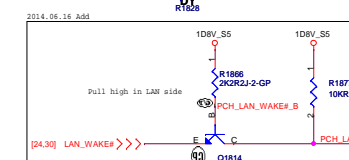
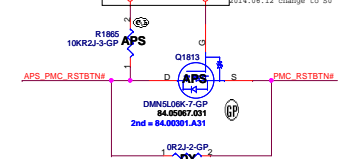
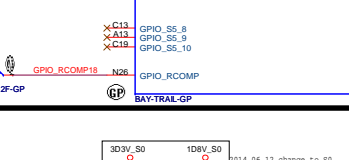
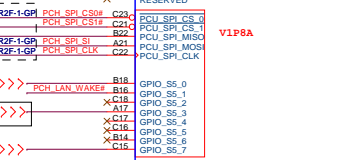
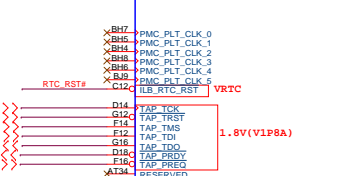
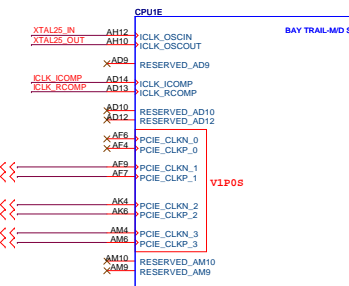
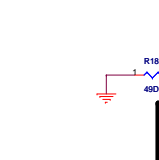
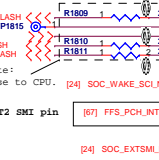
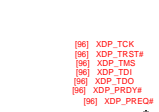
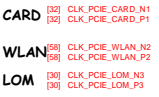
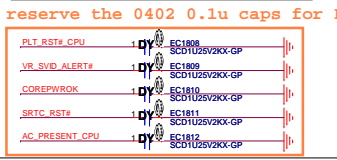
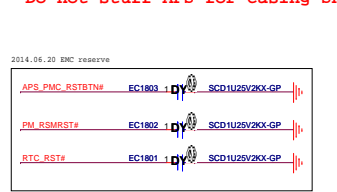
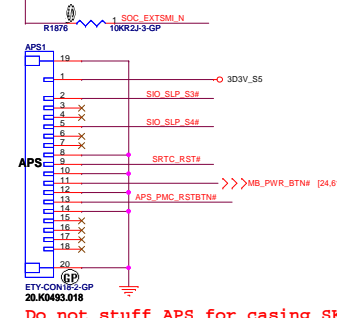
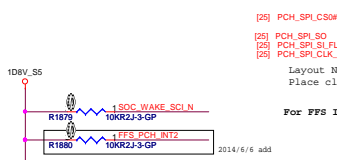
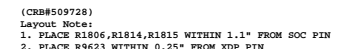
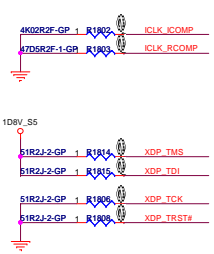
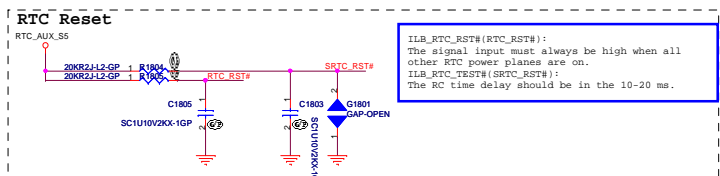
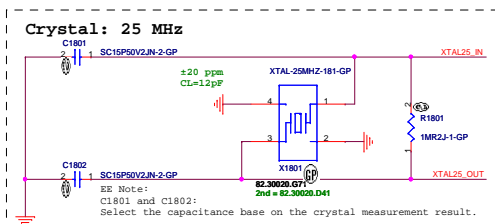
Rev

**A00**

Date: Monday, December 22, 2014

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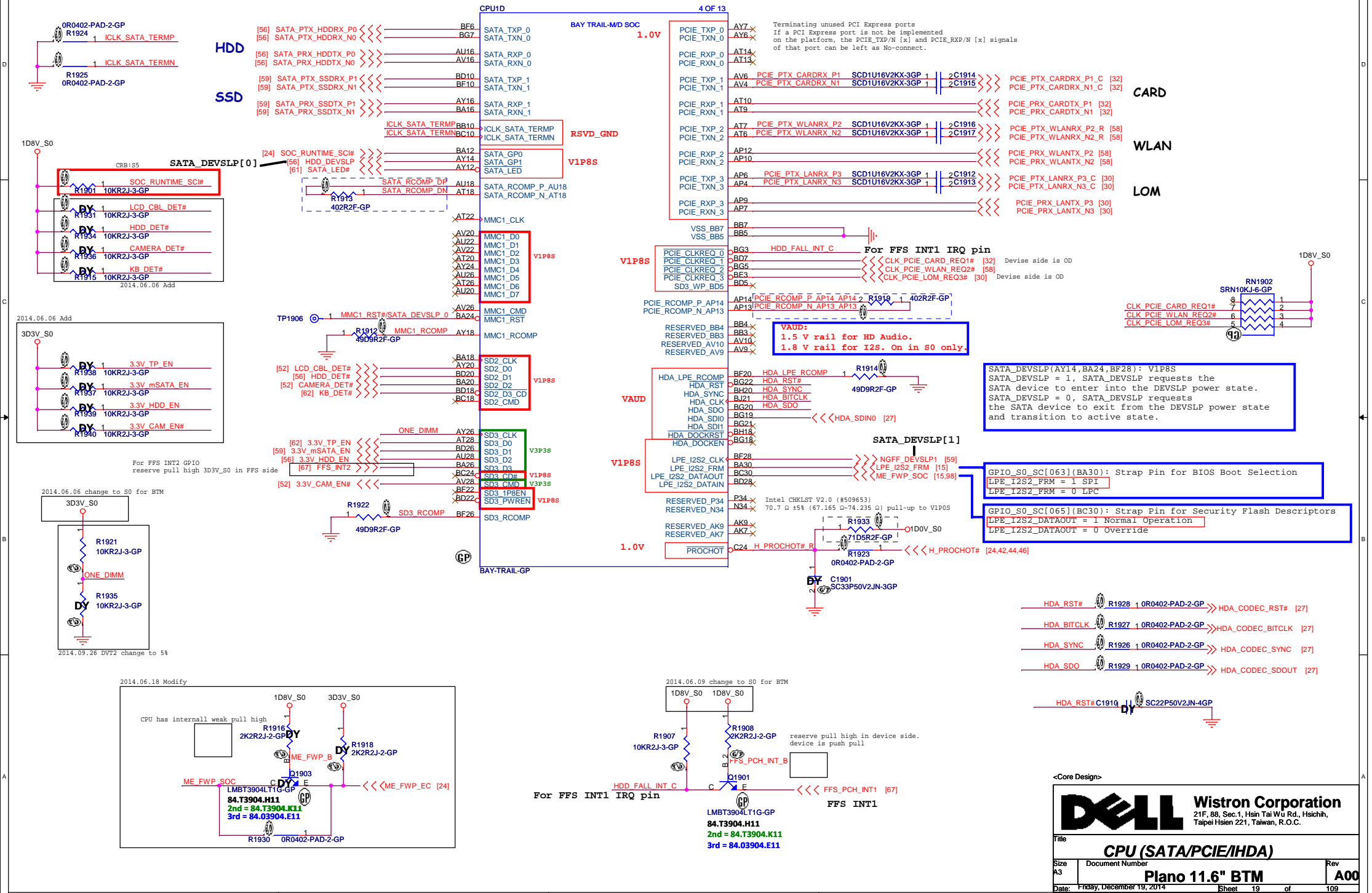
## SSID = PCH



**SSID = PCH**

SATA\_GP:  
When used as an interlock switch status indication, this signal should be driven to '0' to indicate that the switch is closed, and to '1' to indicate that the switch is open.

Root port configurations are set by SoftStraps stored in SPI flash, and the default option is "(4) x1". Links for each root port will train automatically to the maximum possible for each port.




SSID = PCH

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Title

**Reserved**

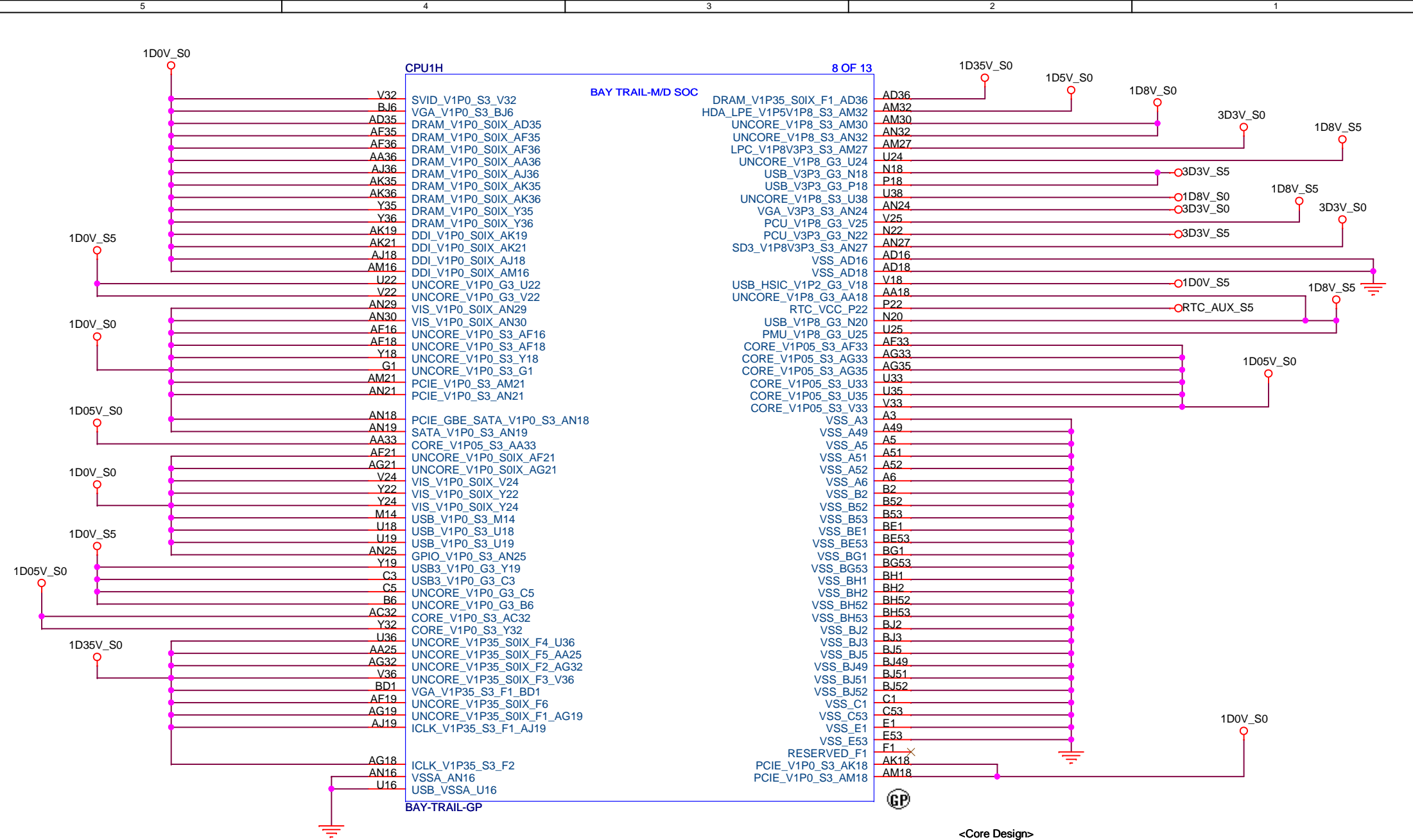
Size  
A4

Document Number  
**Plano 11.6" BTM**

Rev  
**A00**


Date: Tuesday, December 16, 2014

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(#512177/EDS)  
V18: USB\_HSIC\_V1P24\_G3 pin(s) can be connected to V1P0A platform rail if USB HSIC is not used.

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Title		
<b>CPU (POWER1)</b>		
Size	Document Number	Rev
A4	<b>Plano 11.6" BTM</b>	<b>A00</b>
Date:	Tuesday, December 16, 2014	Sheet 21 of 109

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application without get Wistron permission

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Title			
<b>Reserved</b>			
Size A4	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
Date: Tuesday, December 16, 2014		Sheet 22 of	109

SSID = PCH

# Blanking

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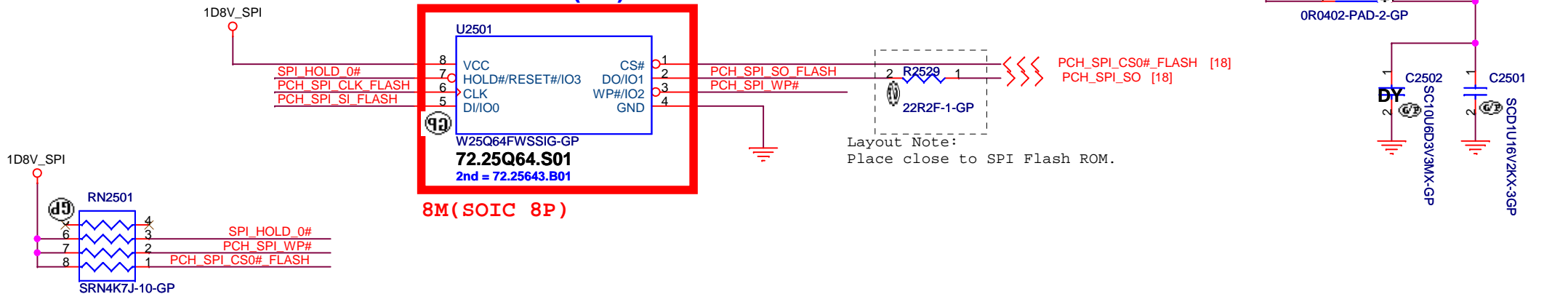
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>CPU (VSS)</b>			
Size A4	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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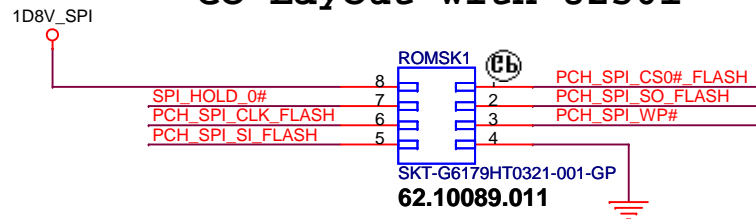


SSID = Flash.ROM

## SYSTEM SPI ROM SPI Flash ROM(8M) for PCH

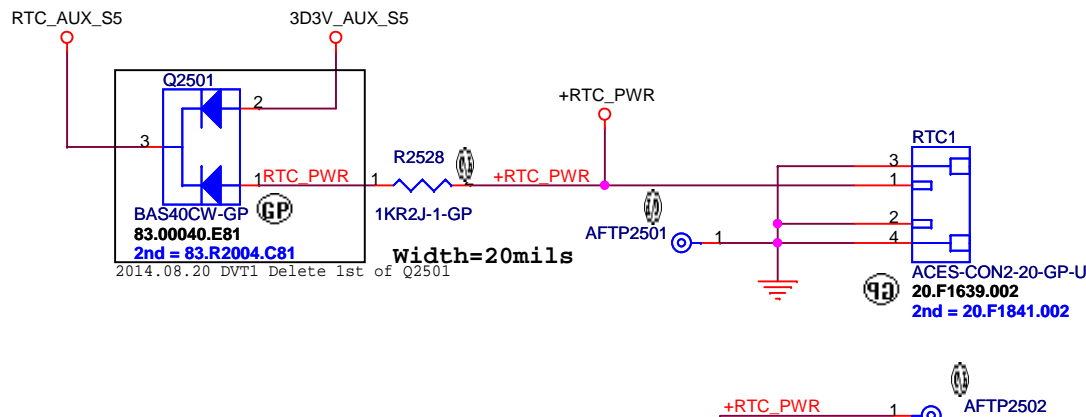


## SPI ROM socket Co-Layout with U2501



Debug config need to stuff socket and SOIC(072.25128.0F01)

SSID = RTC



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Title

**Flash/RTC**

Size  
A4

Document Number

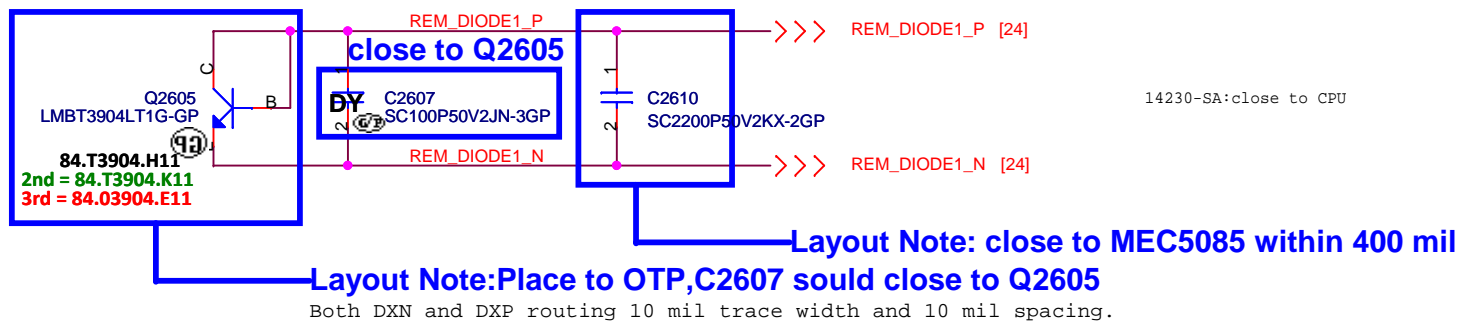
**Plano 11.6" BTM**

Rev  
**A00**

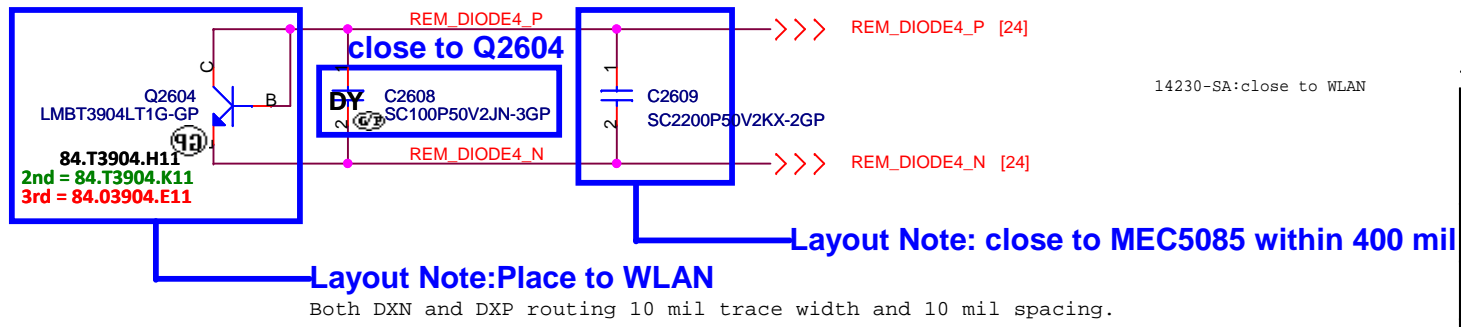
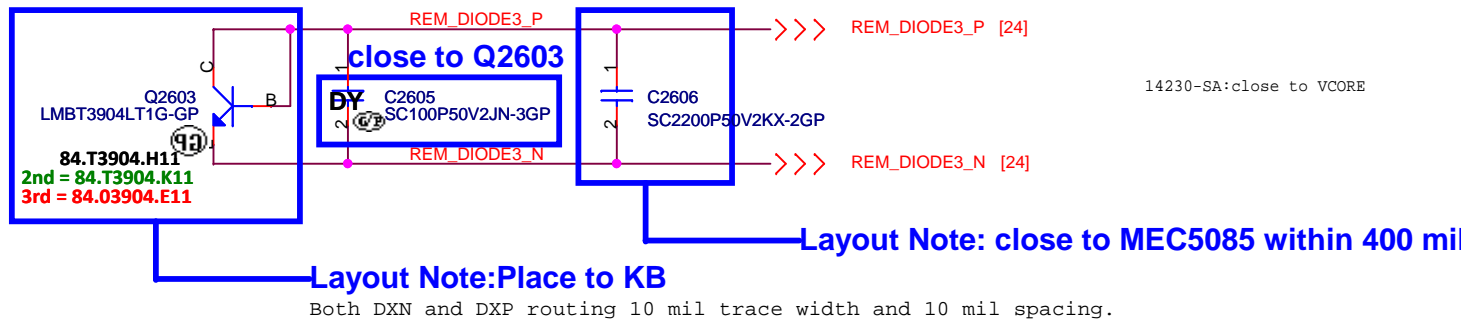
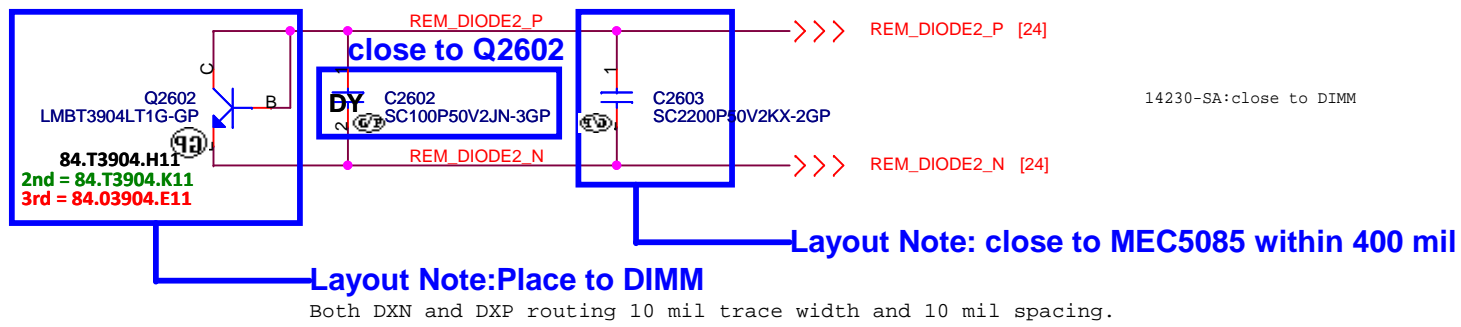
Date: Tuesday, December 16, 2014

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SSID = Thermal



Channel 1 is for CPU  
Channel 2 is for DIMM  
Channel 3 is for KB Skin  
Channel 4 is for WLAN



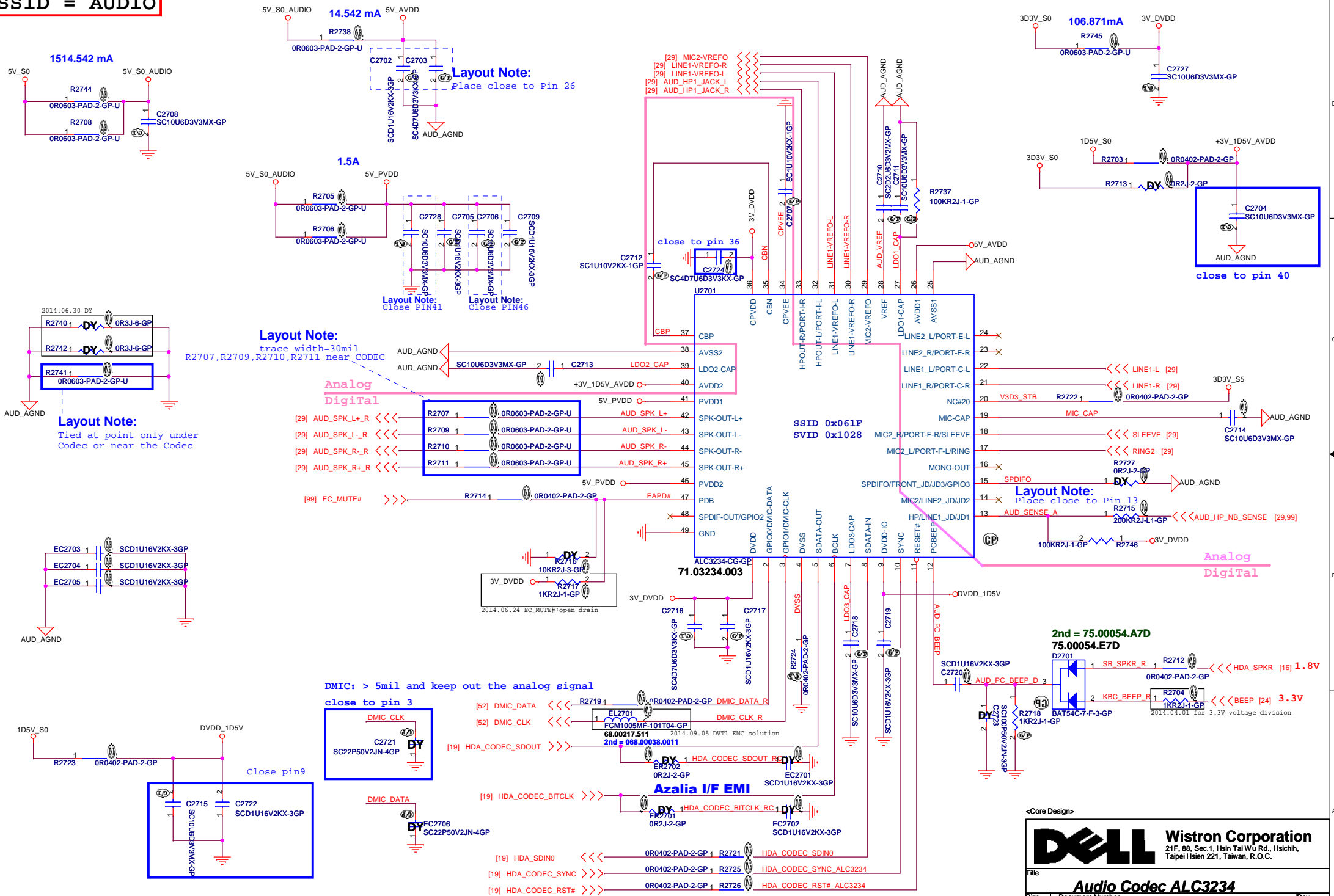
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Title <b>Thermal</b>		
Size A4	Document Number <b>Plano 11.6" BTM</b>	Rev <b>A00</b>
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## SSID = AUDIO



(Blanking)

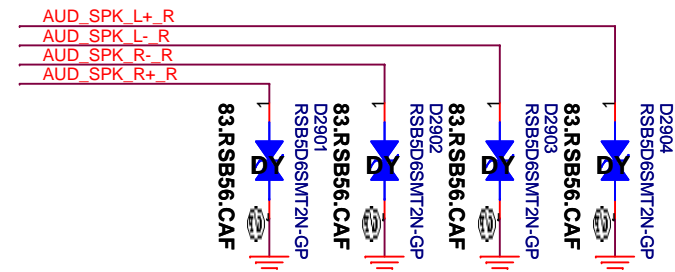
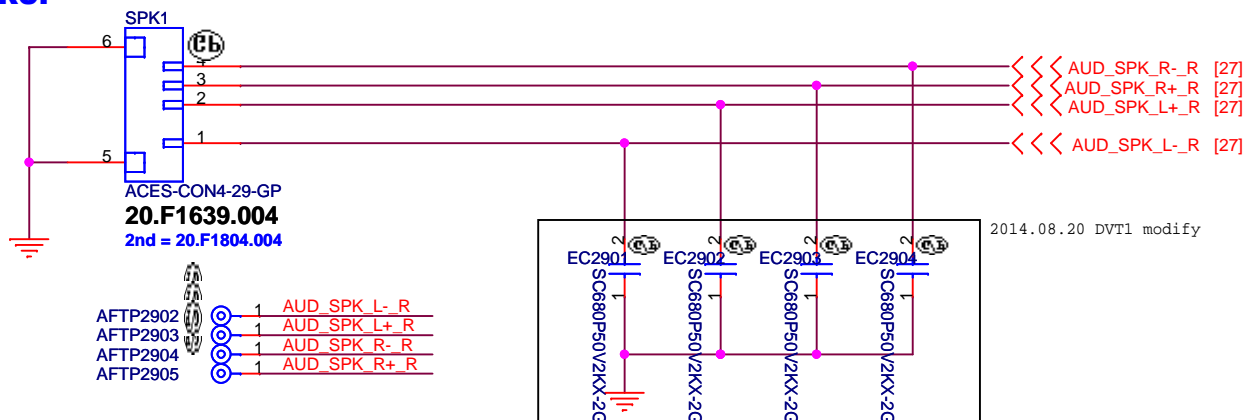
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>			
Size A	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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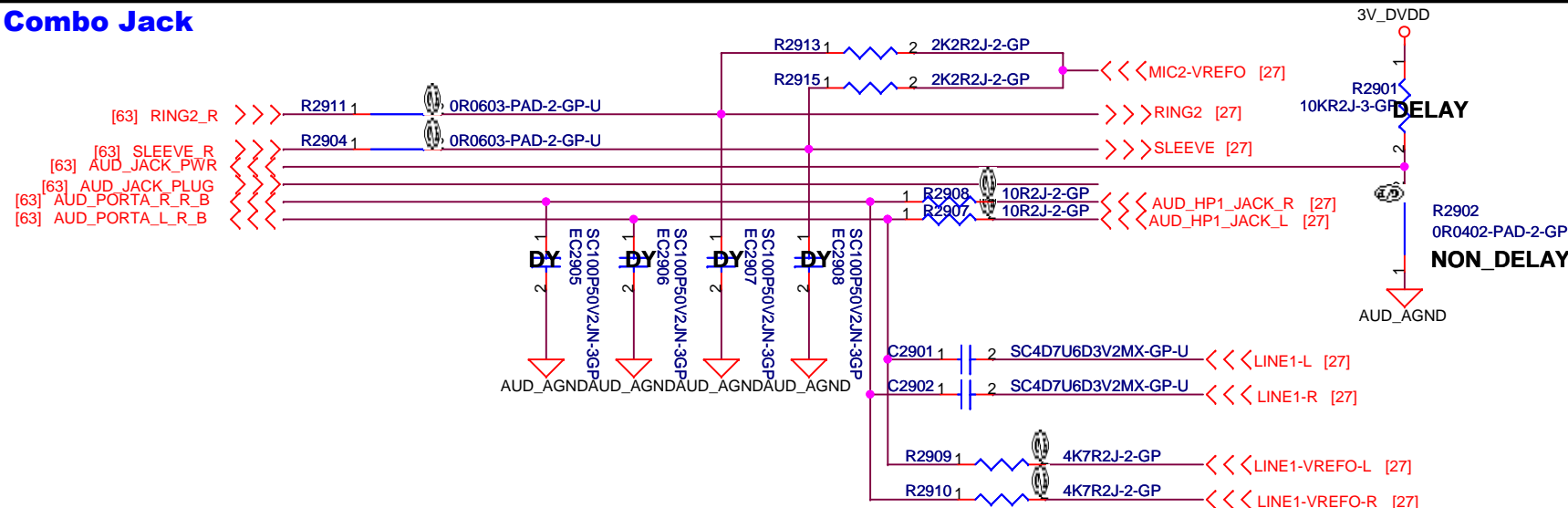
# SSID = AUDIO

## Speaker

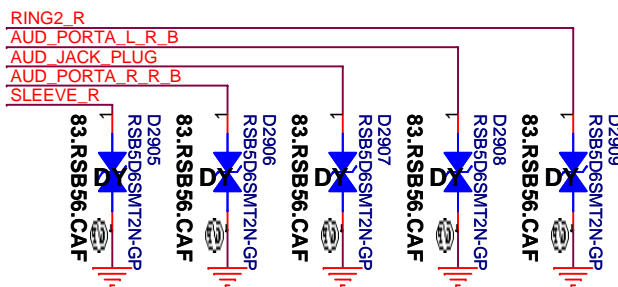
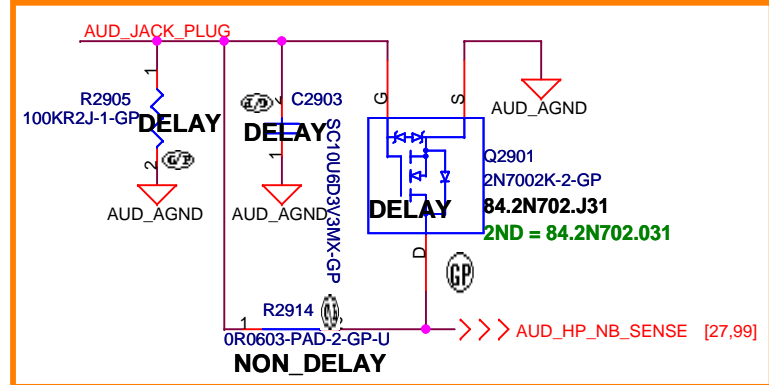
2W/ch



## Combo Jack



## Delay circuit



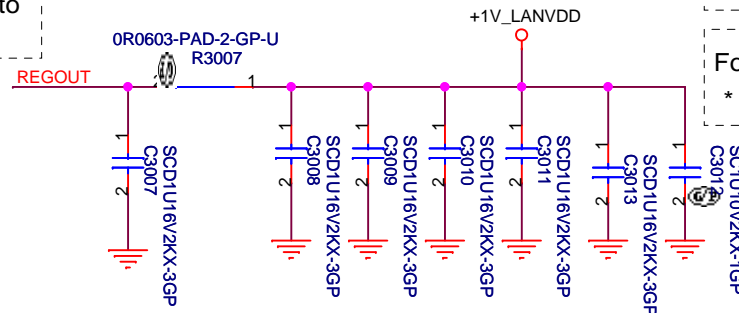
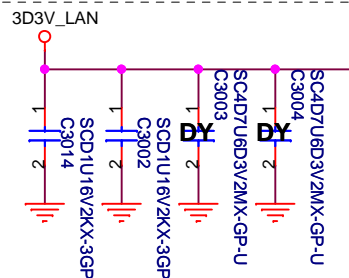
<Core Design>

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Title <b>Speaker/HPMIC CONN</b>		
Size A4	Document Number <b>Plano 11.6" BTM</b>	Rev <b>A00</b>
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# For RTL8151GD

- \* Place C3001 and C3002 close to each AVDD33 pin-- 11, 32
- \* For surge improvement, place C3003 and C3004 close to each AVDD33 pin-- 11, 32. (optional)

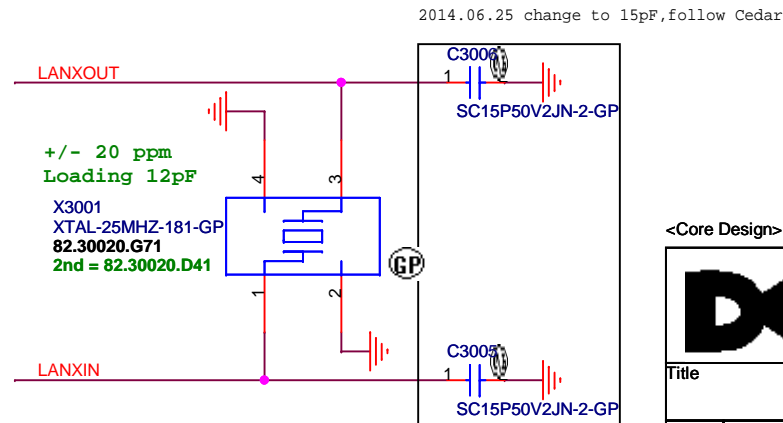
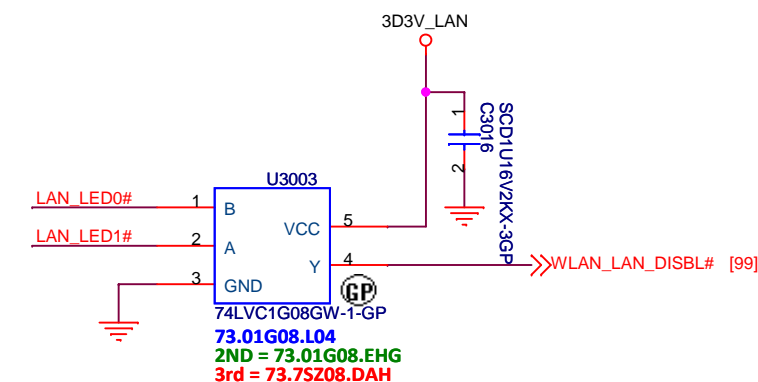
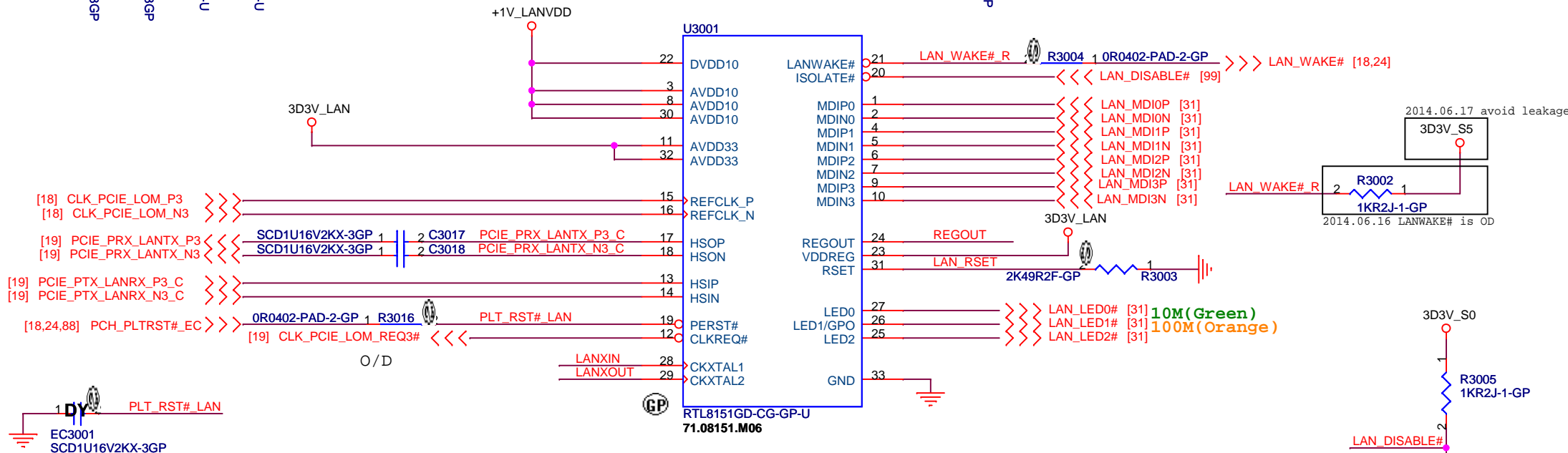


# For RTL8151GD

- \* Place C3008 ~ C3011 close to each VDD10 pin-- 3, 8, 22, 30

# For RTL8151GD

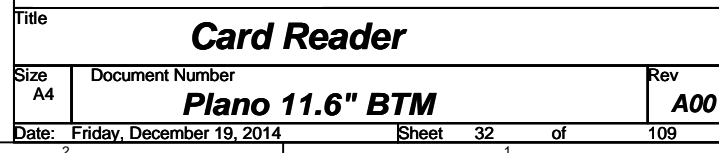
- \* Place C3012 and C3013 close to each VDD10 pin-- 22



<Core Design>

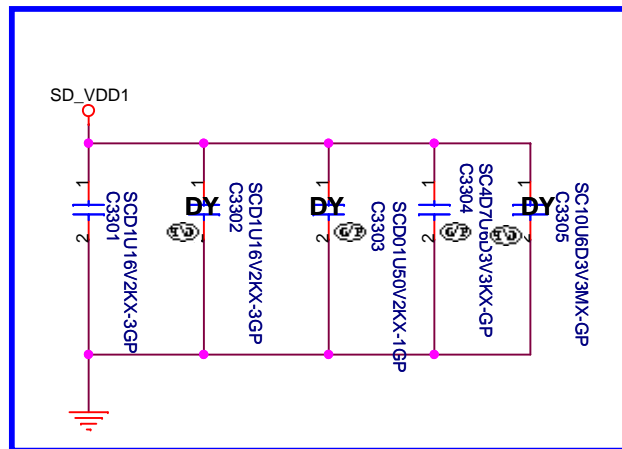
<b>DELL</b>		<b>Wistron Corporation</b>	
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Title <b>LOM RTK8111G</b>			
Size A4	Document Number	Rev A00	
Date: Tuesday, December 16, 2014 Sheet 30 of 109			





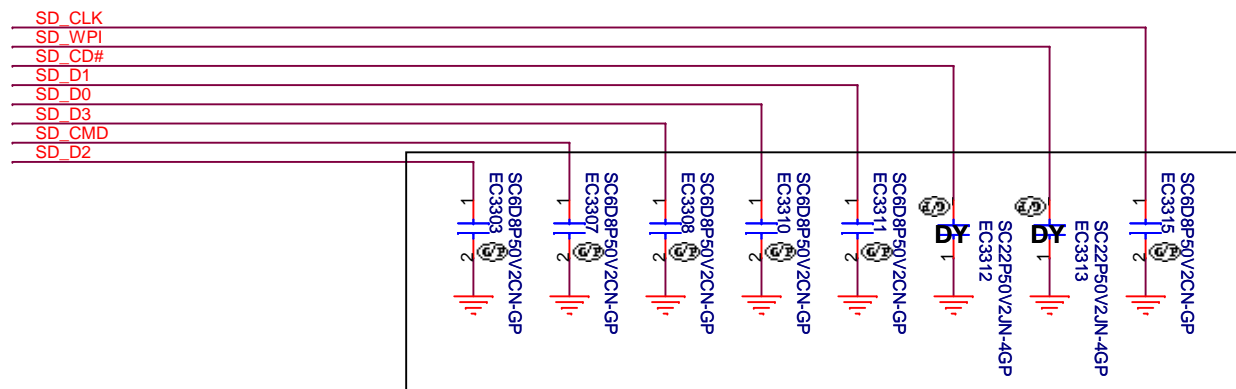
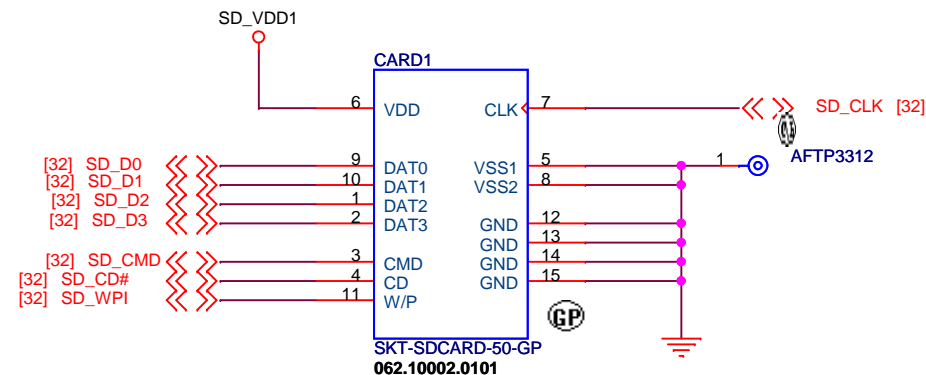


# SSID =Card Reader

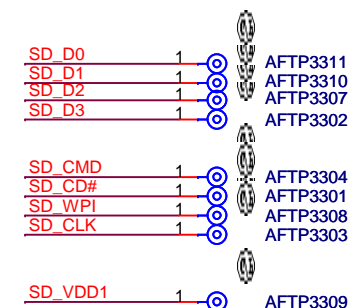


Layout Note:Close to Card Reader CONN

## SD 3.0 Card Connector



C<=10pF 2014/10/30 DVT2 add cap for EMI



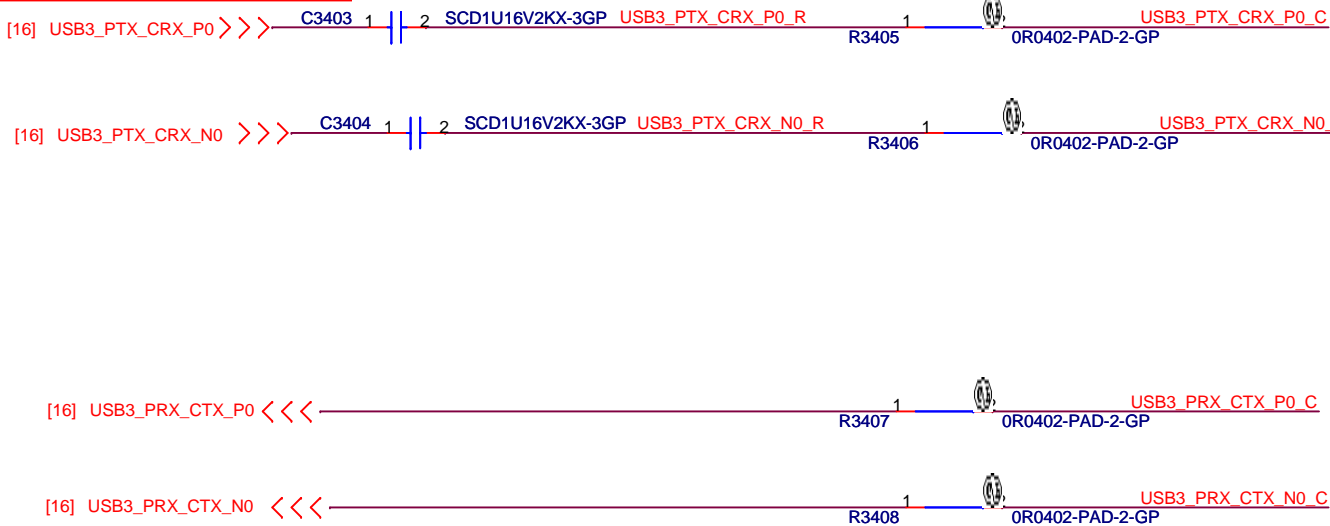
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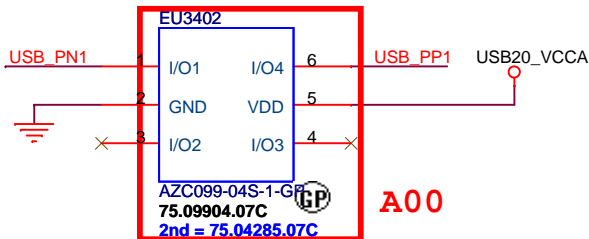
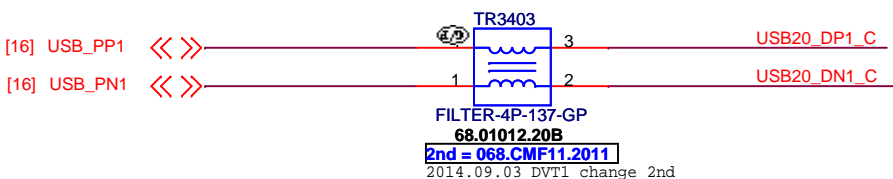
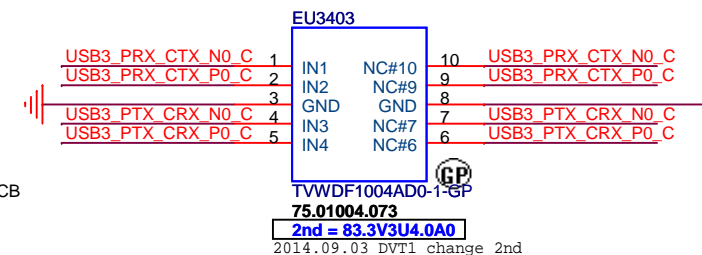
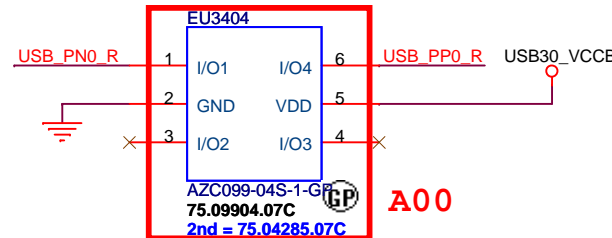
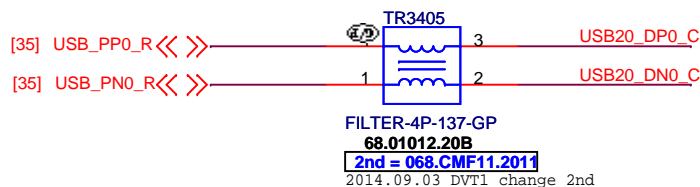
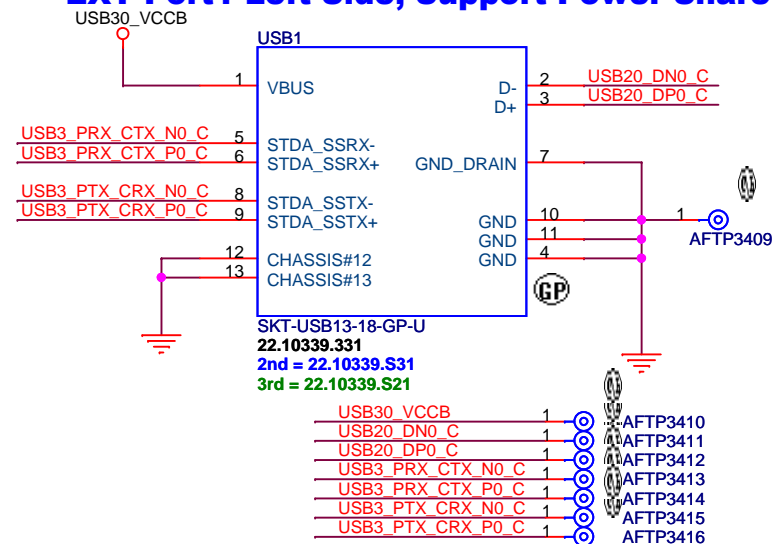
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Title <b>Card Reader CONN</b>		
Size A4	Document Number <b>Plano 11.6" BTM</b>	Rev <b>A00</b>
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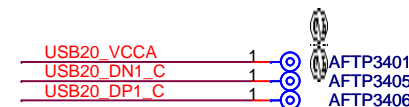
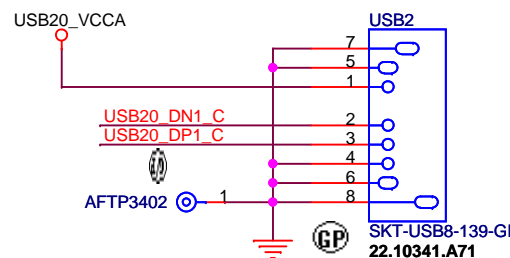
# SSID = USB



## EXT Port1 Left Side, Support Power Share



## EXT Port2 Right Side



<Core Design>

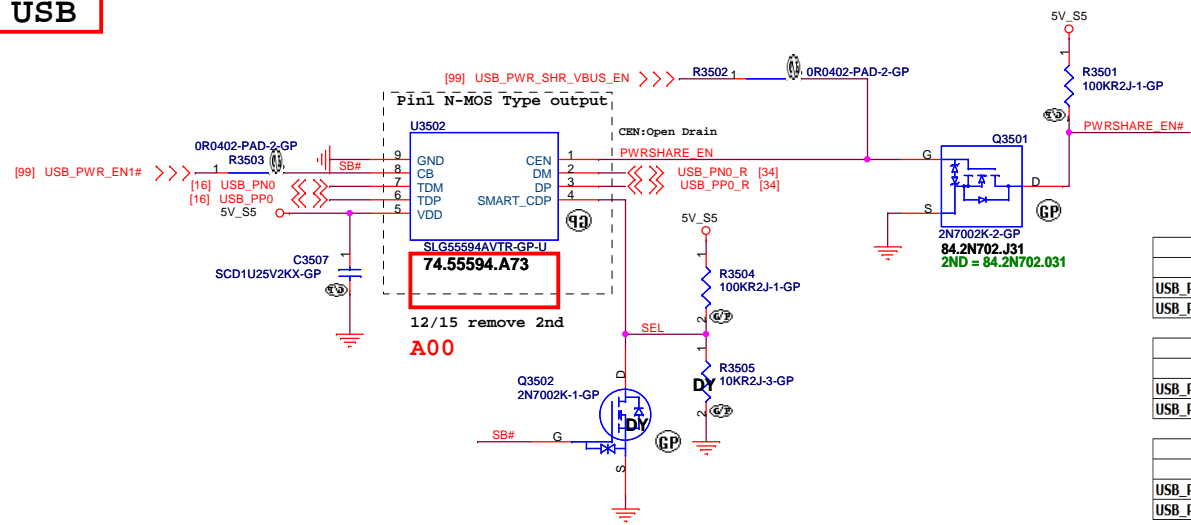


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Title		
USB2.0/3.0/USBHubCONN		
Size	Document Number	Rev
A4	Plano 11.6" BTM	A00
Date:	Monday, December 22, 2014	Sheet 34 of 109

SSID = USB



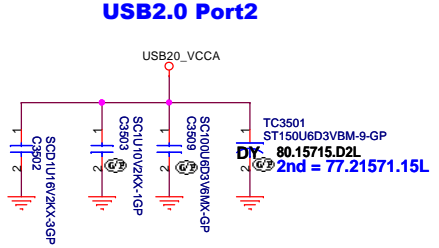
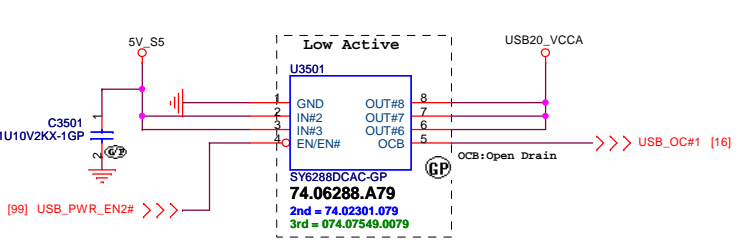
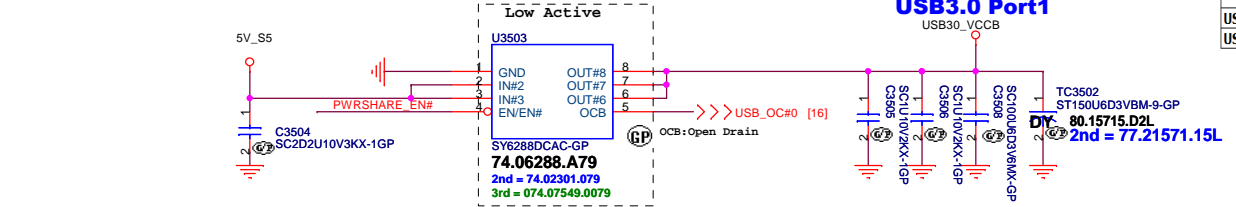
CB	SMART-CDP	Function
0	X	DCP autotdetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device) And, when Non-CDP phone is plugged in, the CDP mode will be changed automatically to SDP mode during handshaking protocol for supporting data communication.

AC mode					DC mode				
Feature Enable/USB wake Enable					Feature Enable/USB wake Enable				
S0	S3	S4	S5		S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0	USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	1	1	1	USB_PWR_SHR_VBUS_EN (Charge)	1	1	0	0

Feature Enable/USB wake Disable					Feature Enable/USB wake Disable				
S0	S3	S4	S5		S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0	USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	1	1	1	USB_PWR_SHR_VBUS_EN (Charge)	1	1	0	0

Feature Disable/USB wake Enable					Feature Disable/USB wake Enable				
S0	S3	S4	S5		S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0	USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	1	0	0	USB_PWR_SHR_VBUS_EN (Charge)	1	1	0	0

Feature Disable/USB wake Diable					Feature Disable/USB wake Diable				
S0	S3	S4	S5		S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0	USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	0	0	0	USB_PWR_SHR_VBUS_EN (Charge)	1	0	0	0



USB Power SW (U3501 & U3503)


Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.079	2ND



SSID = Reset.Suspend


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Title			
<b><i>RUN POWER</i></b>			
Size A4	Document Number <b><i>Plano 11.6" BTM</i></b>		Rev <b><i>A00</i></b>
Date: Tuesday, December 16, 2014		Sheet 37 of	109

( Blanking )

<Core Design>

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Title <b>Reserved</b>			
Size A4	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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Size A	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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SSID = OBFF

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Title <b>Reserved</b>			
Size A4	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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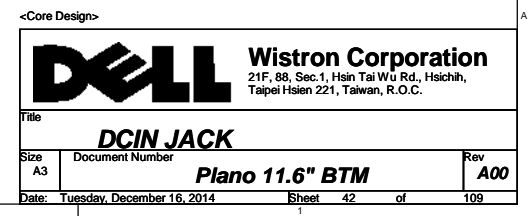
( Blanking )

<Core Design>

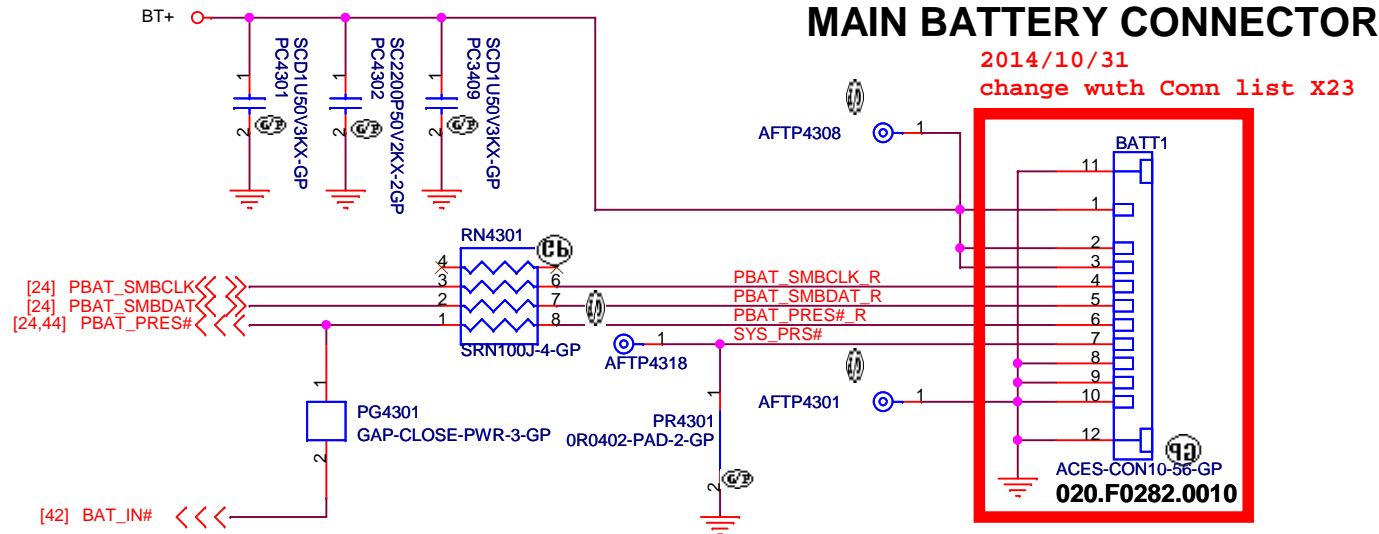
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Title <b>Reserved</b>			
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**0103 Add EC4203**  
ndde close to EL4202

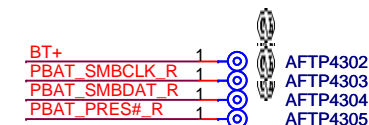
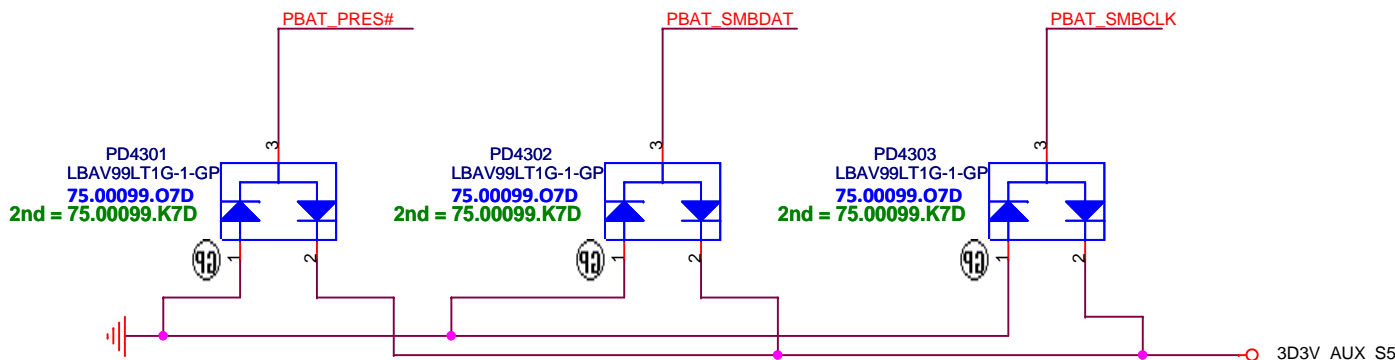
**Layout Note:**  
PSID Layout width > 25mil



SSID = PWR.Support



**Layout Note:** Place near Battery CONN



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Title

**BATTERY CONN**

Size  
A4

Document Number

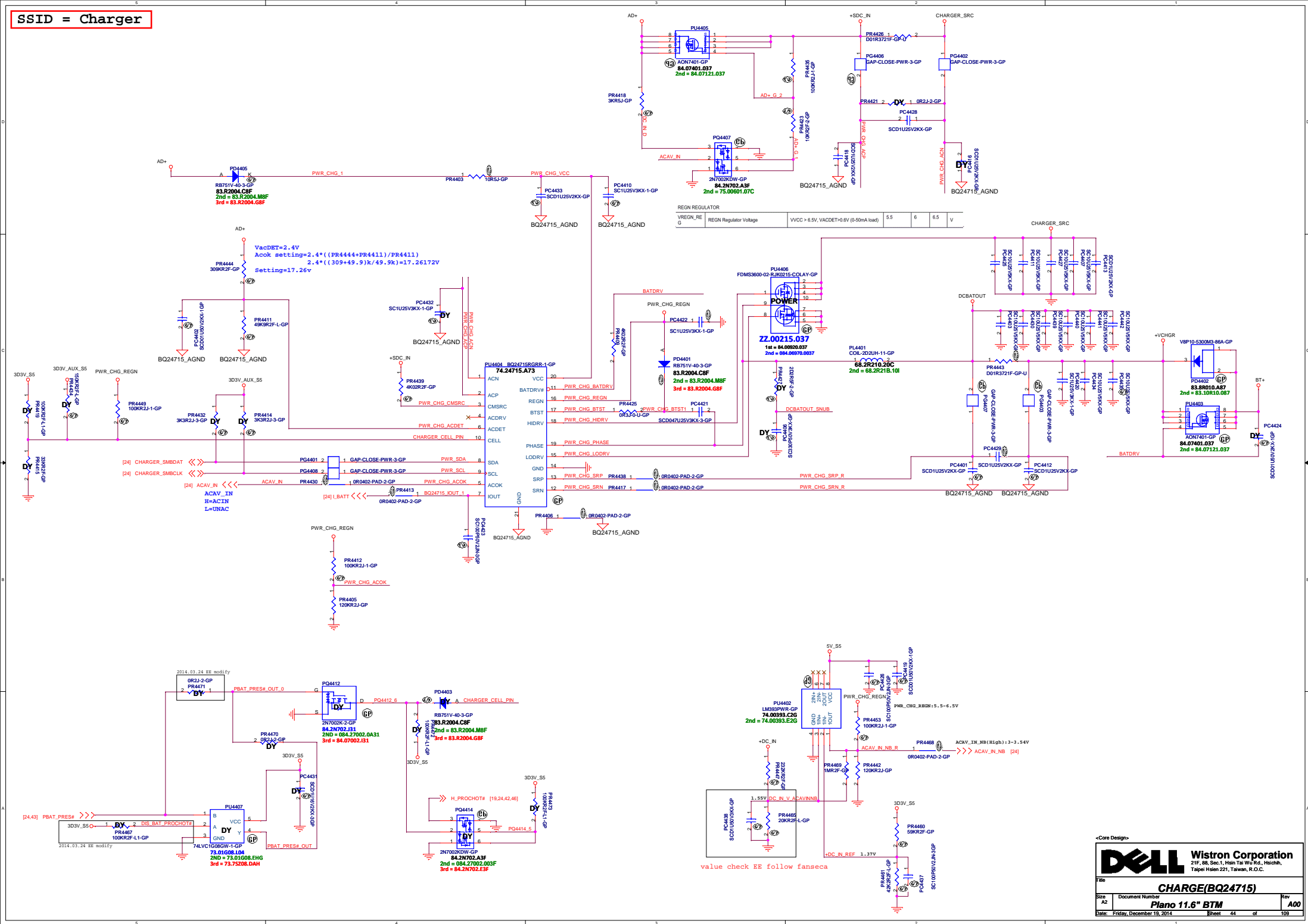
**Plano 11.6" BTM**

Rev  
A00

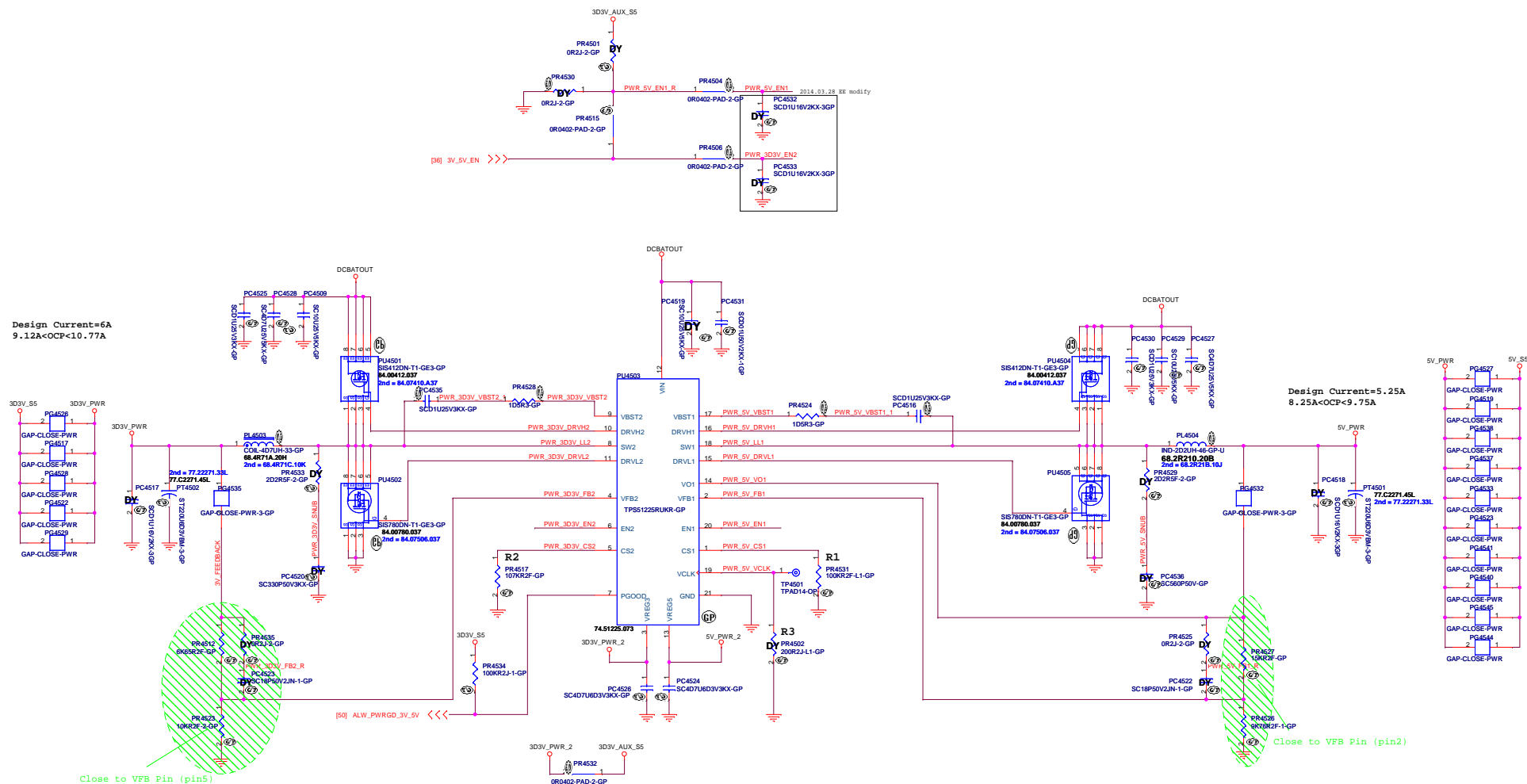
Date: Tuesday, December 16, 2014

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SSID = Charger

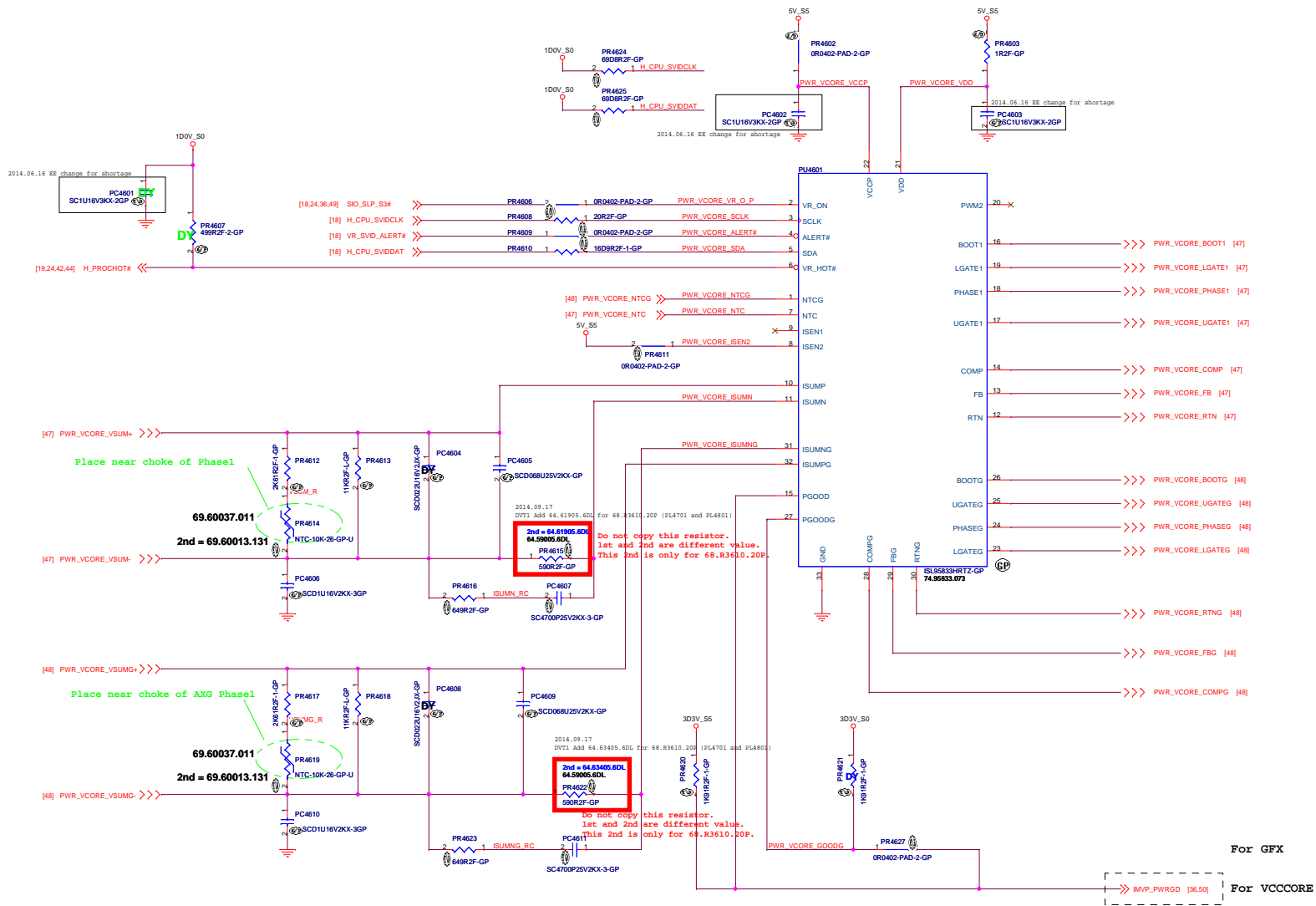


SSID = PWR.Plane.Regulator\_5v3p3v

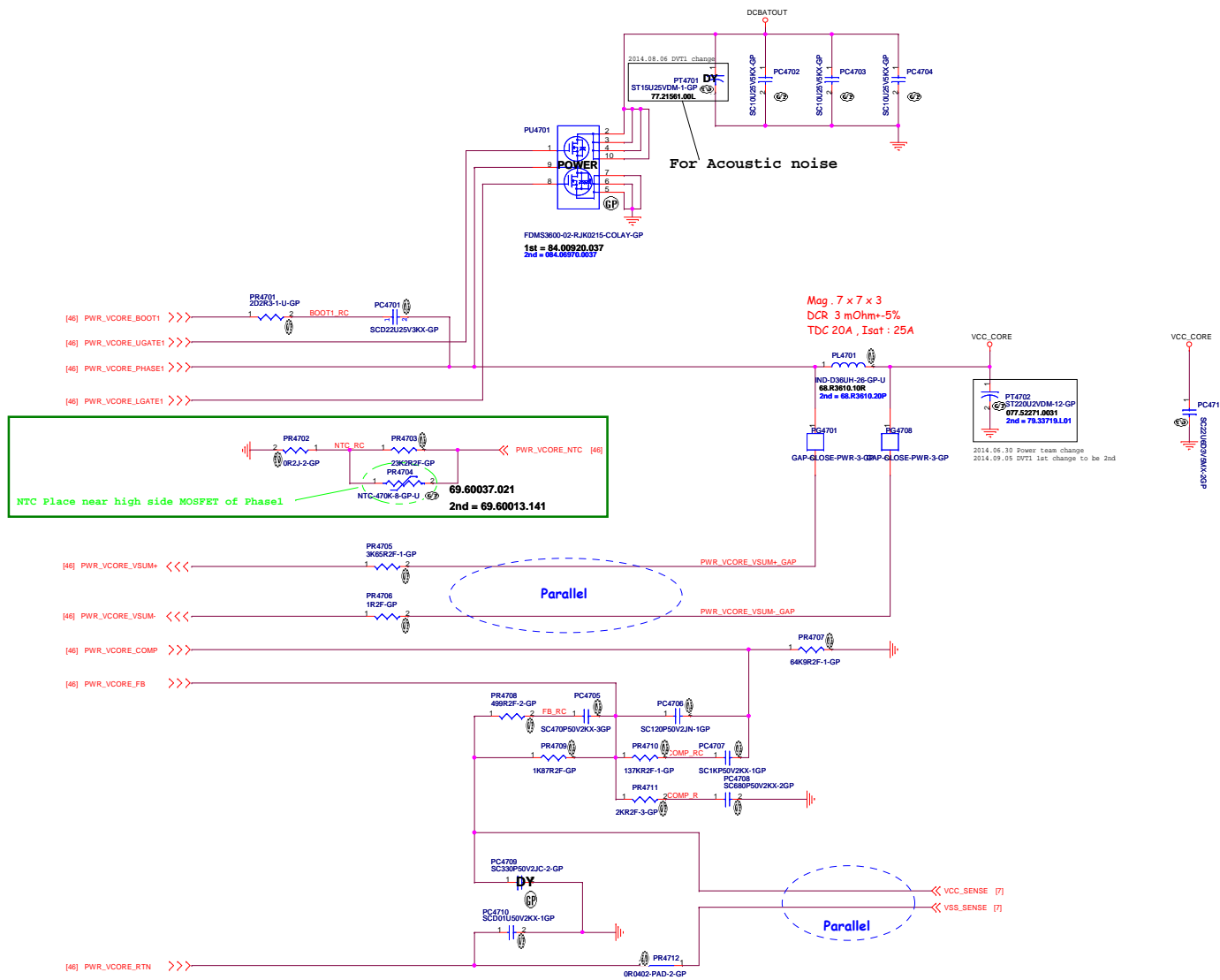


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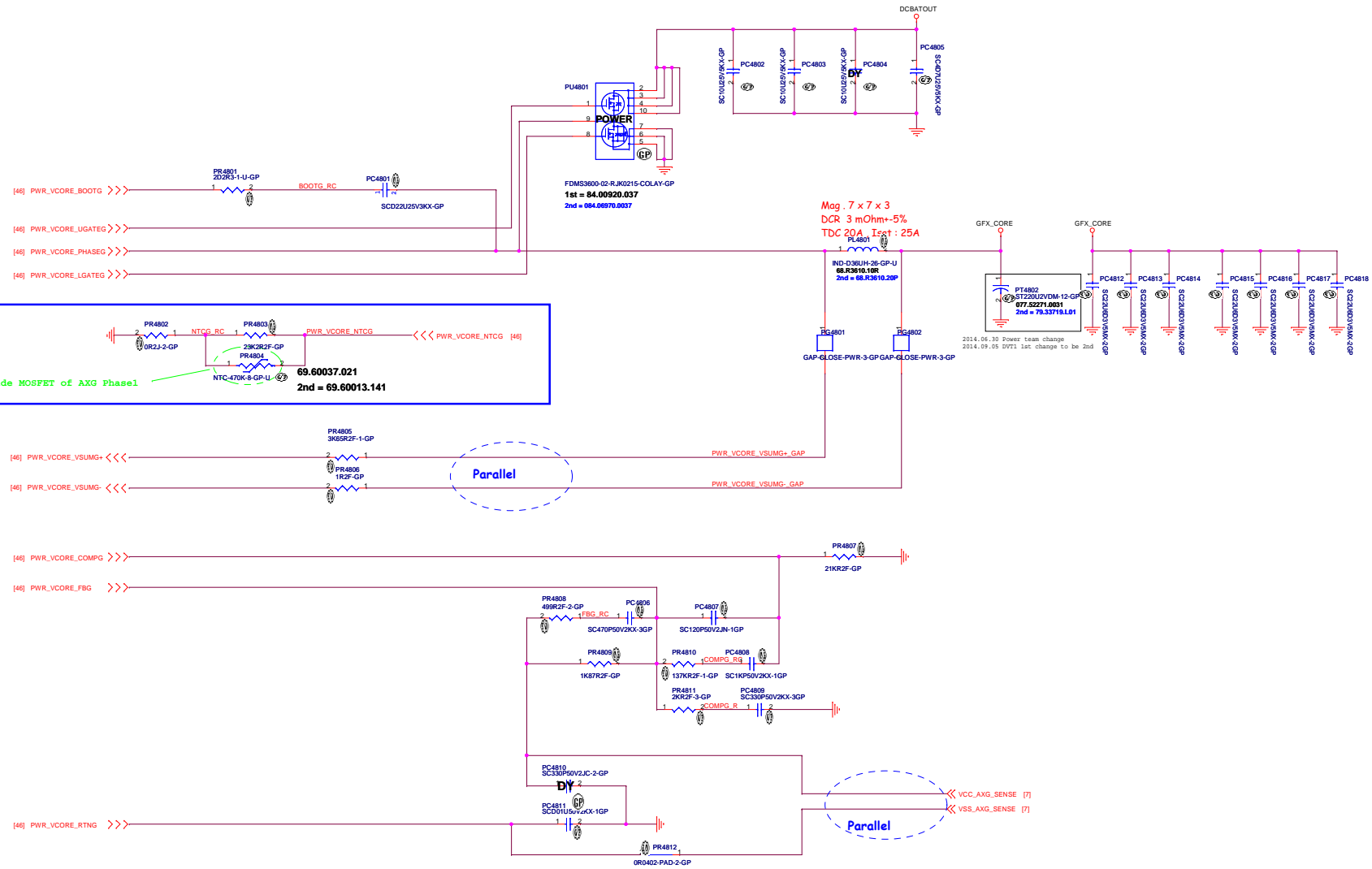
SSID = CPU Regulator



# SSID = CPU Regulator

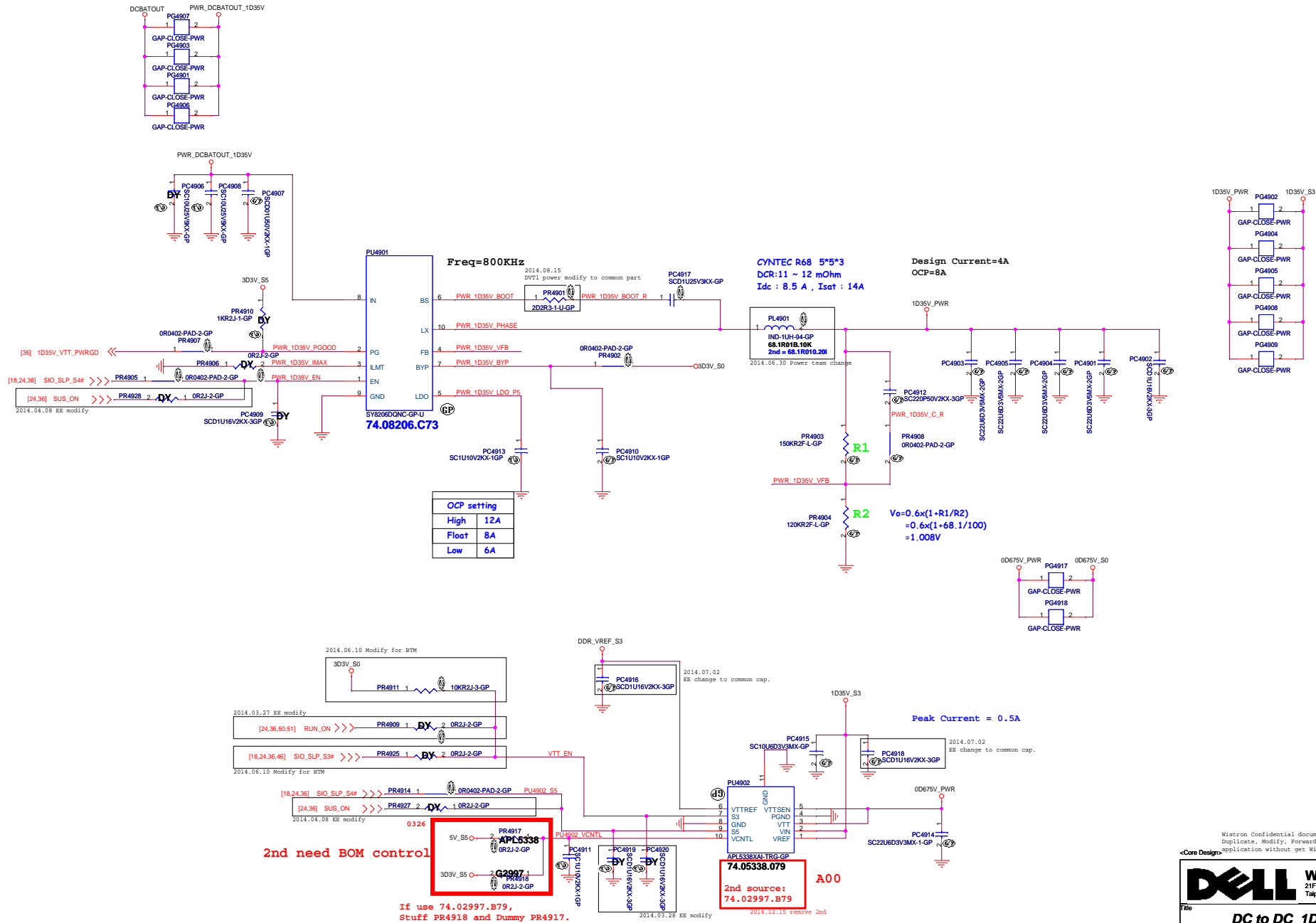


# SSID = GFX Regulator





# SY8206D for 1D35V



## ***SY8206D for 1D0V\_S5***



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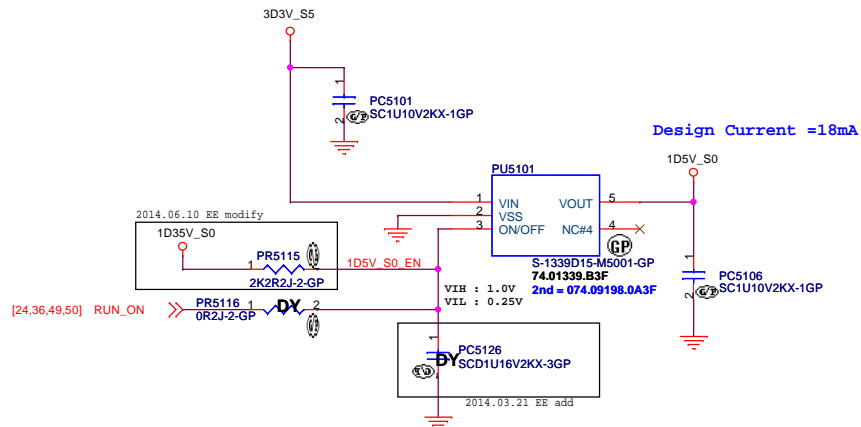
**DCDC 1D05V 1D0V**

### Plano 11.6" BTM

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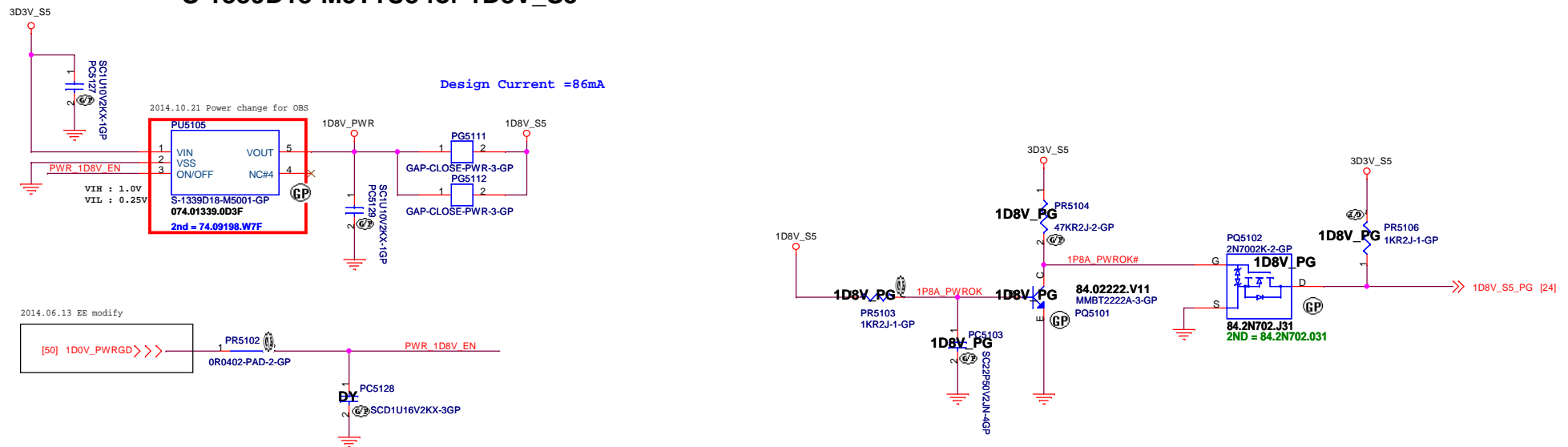
```
SSID = PWR.Plane.Regulator_1p5v
```

**S-1339D15-M5001 for 1D5V\_S0**



```
SSID = PWR.Plane.Regulator_1p8v
```

**S-1339D18-M5T1U3 for 1D8V\_S5**



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Title	Author	Year	Journal	Volume	Page
...	...	...	...	...	...

**1D8V\_1D5V**

Size  
A3

Document Number	
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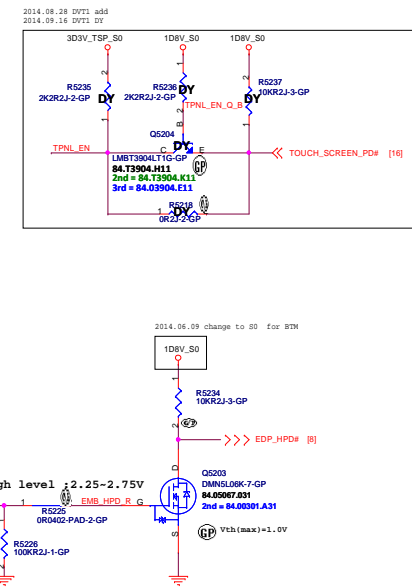
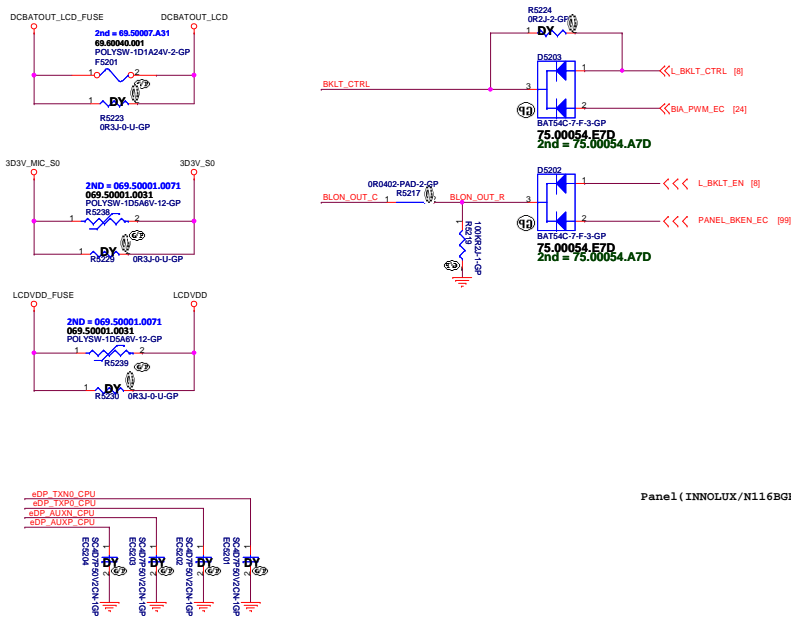
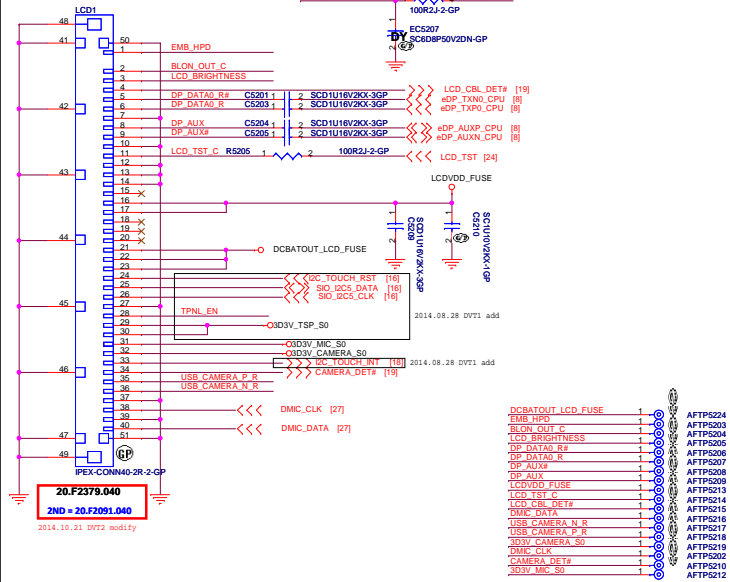
## Plano 11.6" BTM

ev  
A00

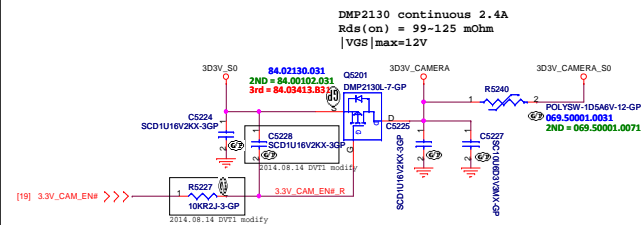
Date: Tuesday, December 16, 2014

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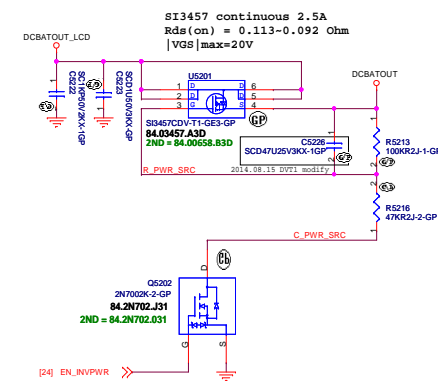
## eDP CONNECTOR



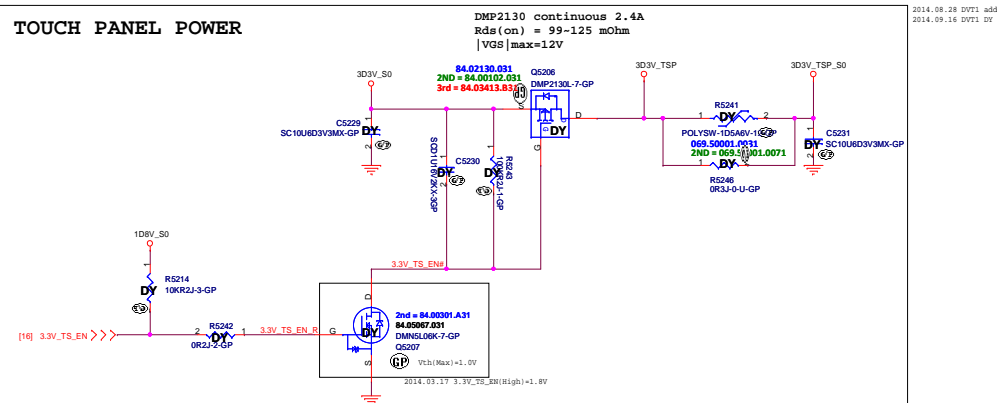
## Camera Power



## INVERTER POWER




TOUCH PANEL POWER



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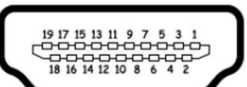
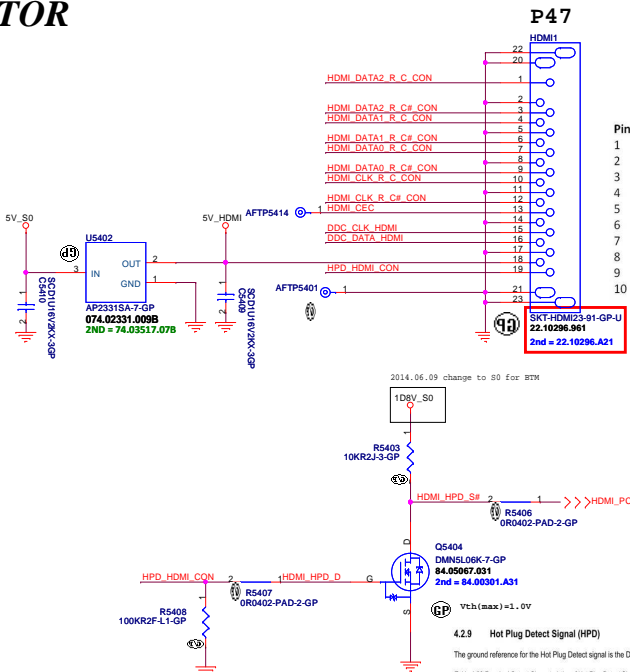
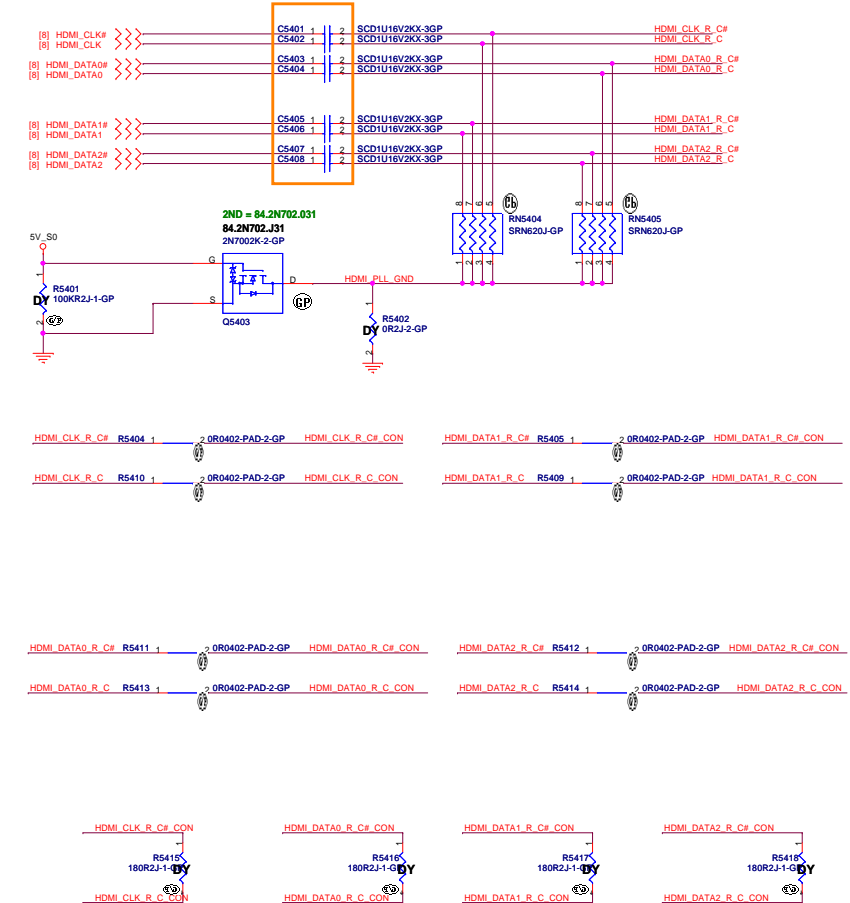
Title

(Reserved)

Size A3	Document Number <b>Plano 11.6" BTM</b>	Rev <b>A00</b>
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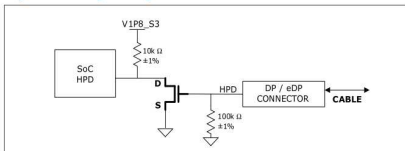
HDMI CONNECTOR

Close to HDMI Connector



Pin#	Signal	Pin#	Signal
1	TMDS data 2+	11	TMDS clock shield
2	TMDS data 2 shield	12	TMDS clock-
3	TMDS data 2-	13	CEC
4	TMDS data 1+	14	No connected
5	TMDS data 1 shield	15	DDC clock
6	TMDS data 1-	16	DDC data
7	TMDS data 0+	17	Ground
8	TMDS data 0 shield	18	+5V power
9	TMDS data 0-	19	Hot plug detect
10	TMDS clock+		

A00



NOTE: It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage <=1.5V.  
NOTE: The HPD PU resistor tolerance can be relaxed to 5%.

4.2.9 Hot Plug Detect Signal (HPD)

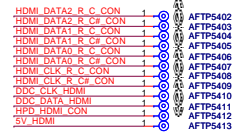
The ground reference for the Hot Plug Detect signal is the DDC/CEC Ground pin.

Table 4-38 Required Output Characteristics of Hot Plug Detect Signal

Item	Value
High voltage level (Sink)	Minimum 2.4 Volts, Maximum 5.3 Volts
Low voltage level (Sink)	Minimum 0 Volts, Maximum 0.4 Volts
Output resistance	1000 ohms <20%

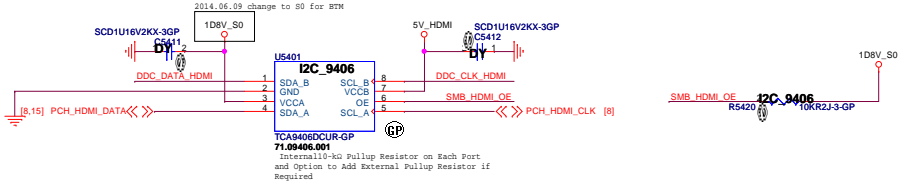
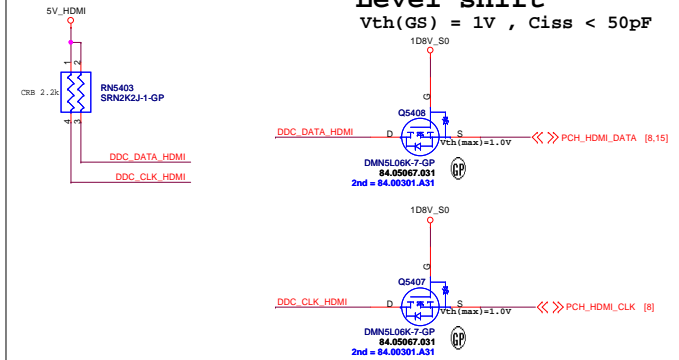
Table 4-39 Required Detection Levels for Hot Plug Detect Signal

Item	Value
High voltage level (Source)	Minimum 2.0 Volts, Maximum 5.3 Volts
Low voltage level (Source)	Minimum 0 Volts, Maximum 0.8 Volts



2014.06.09 Modify for BTM

Level shift  
Vth(GS) = 1V , Ciss < 50pF




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HDMI Level Shifter/Connector

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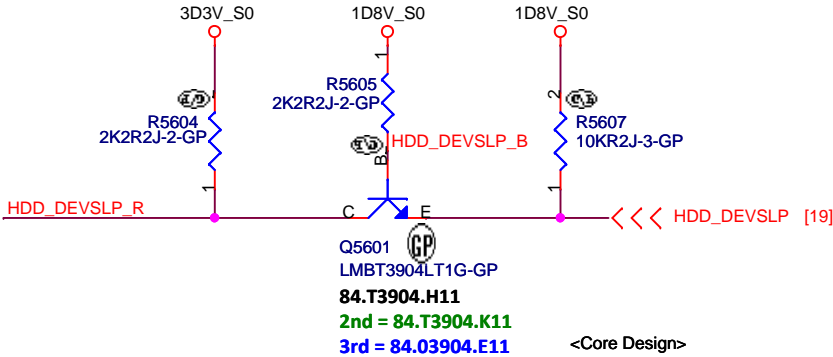
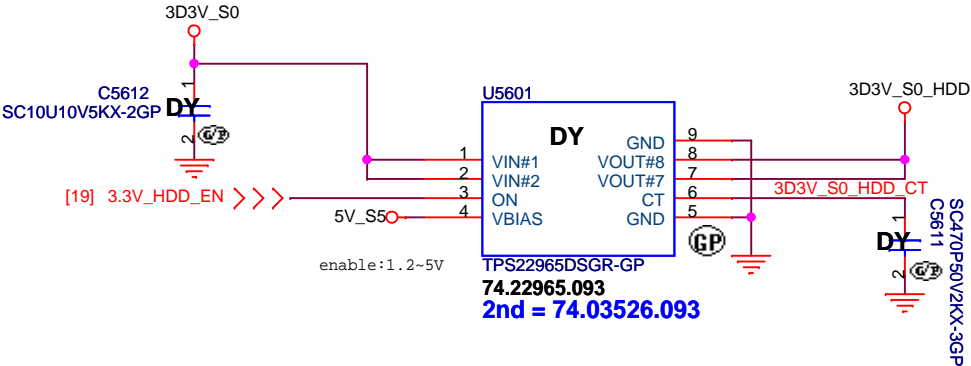
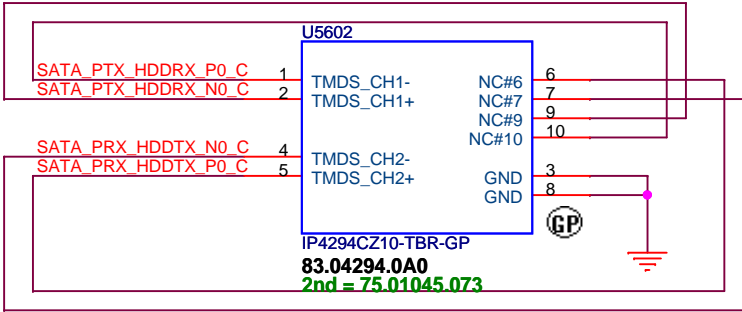
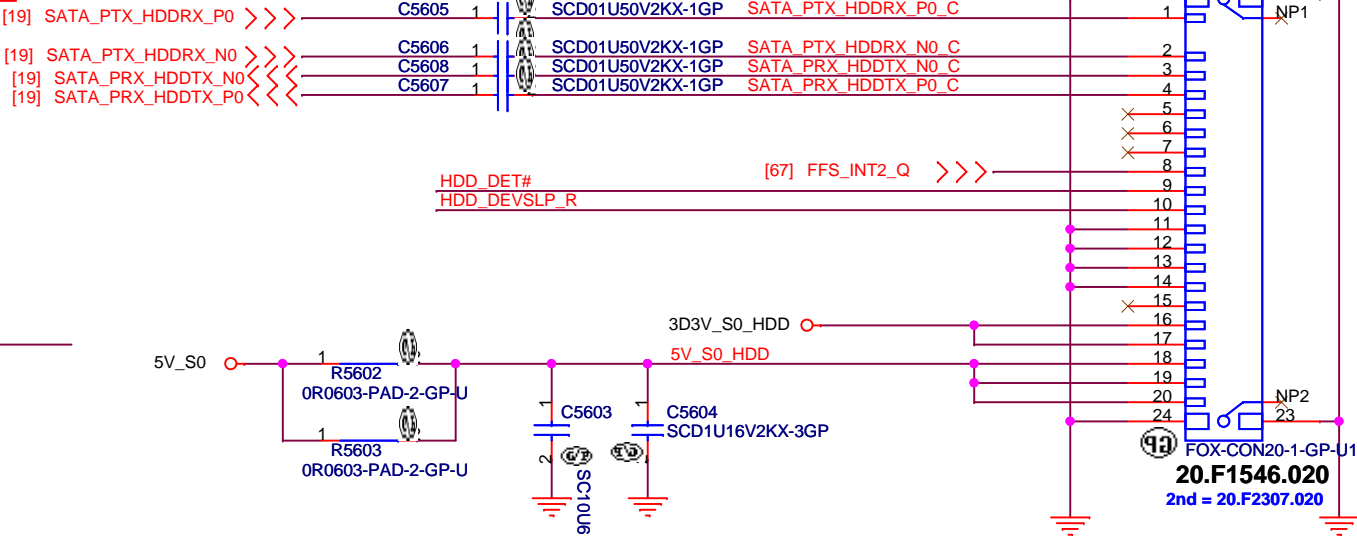
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SSID = SATA




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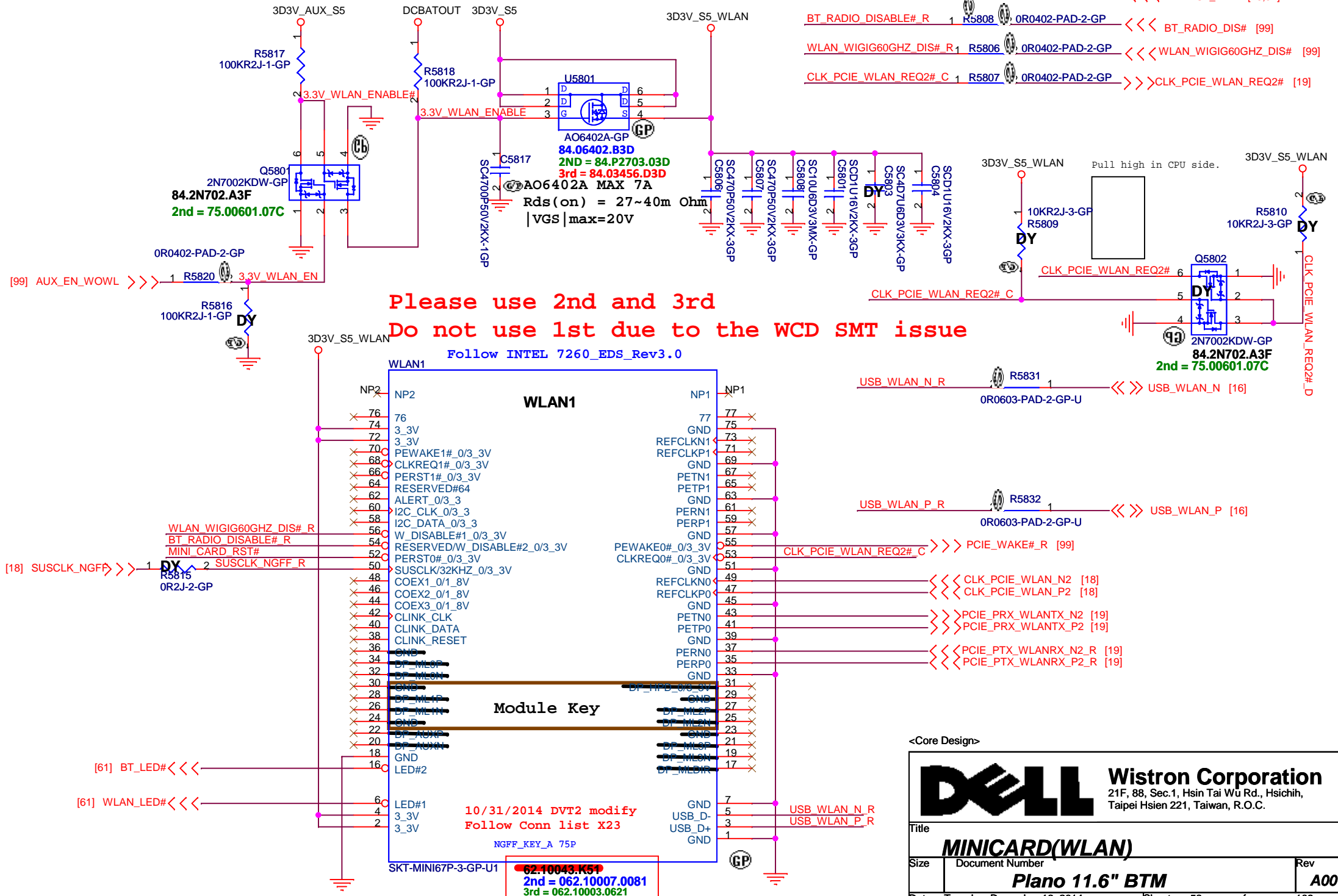


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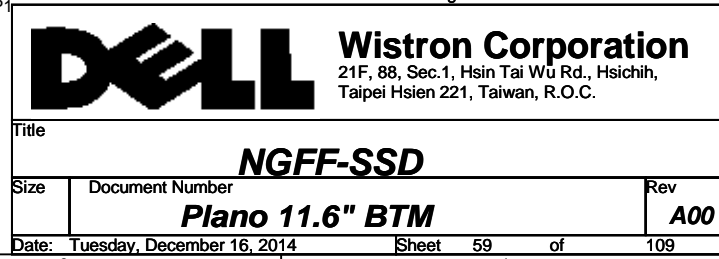
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Title			
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Size A4	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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# SSID = WIRELESS



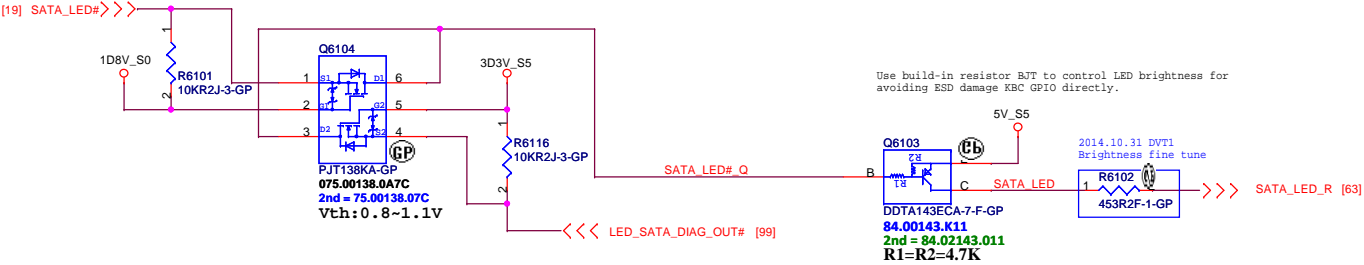
# NGFF SSD



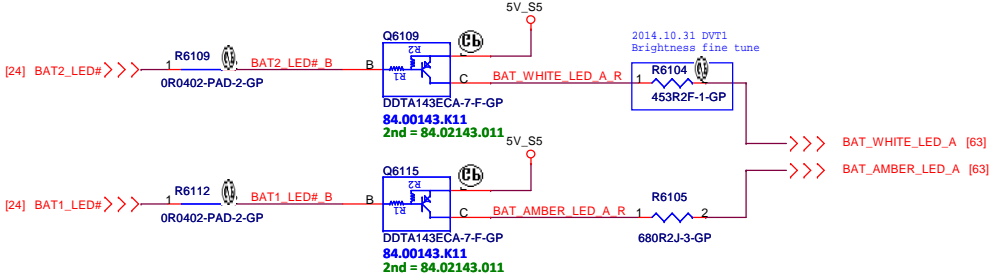


# SSID = User.Interface

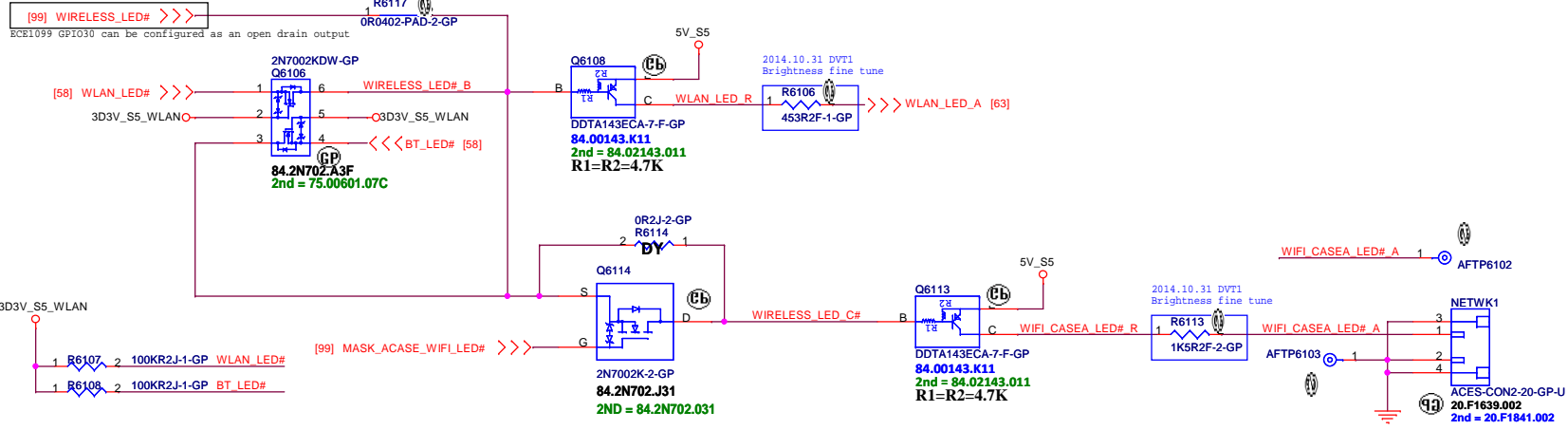
## SATA HDD LED LOW activated from PCH GPIO



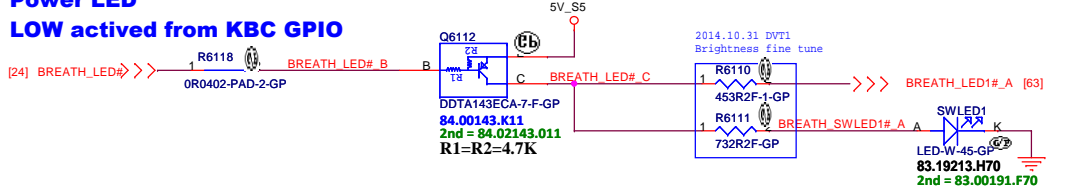
## Battery LED2(White\_LED) LOW activated from KBC GPIO



## WLAN LED LOW activated from KBC GPIO

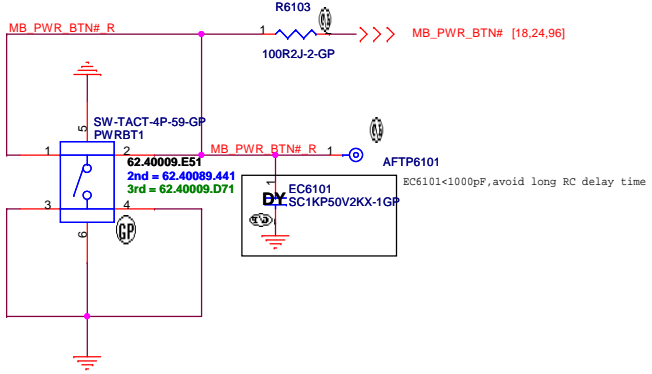


## Power LED LOW activated from KBC GPIO



## POWER BUTTON LED

## POWER BUTTON



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Title

Size

Document Number

Plano 11.6" BTM

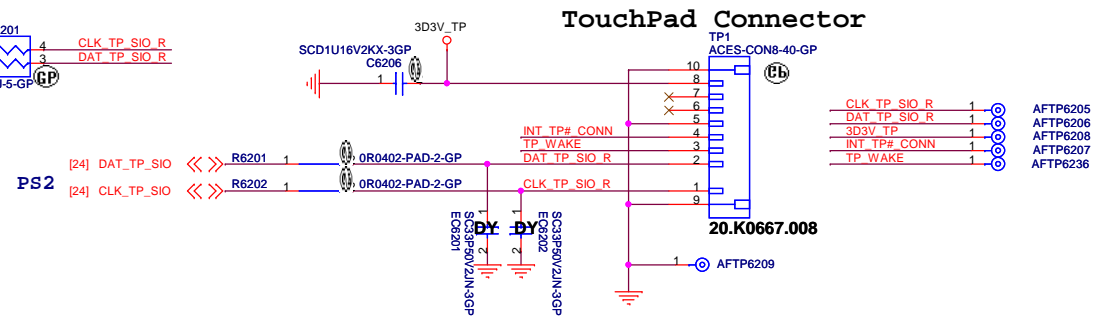
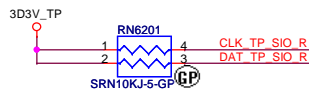
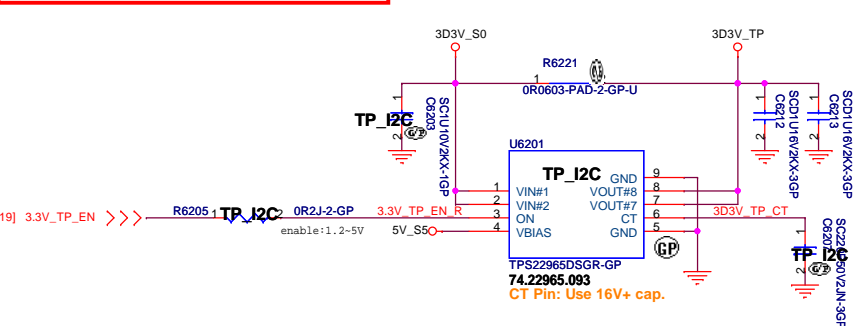
Rev

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Date: Tuesday, December 16, 2014

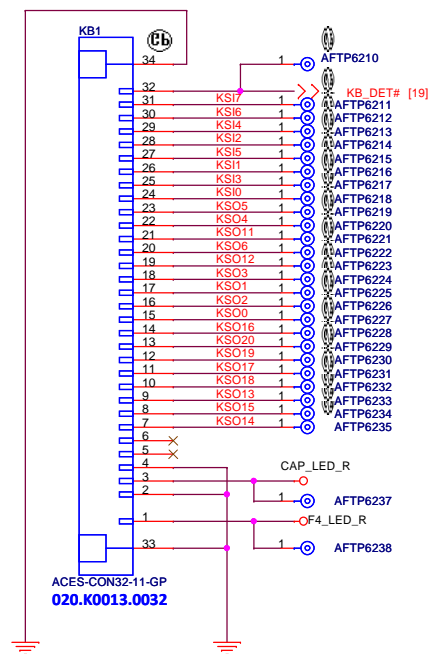
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# SSID = Touch.Pad

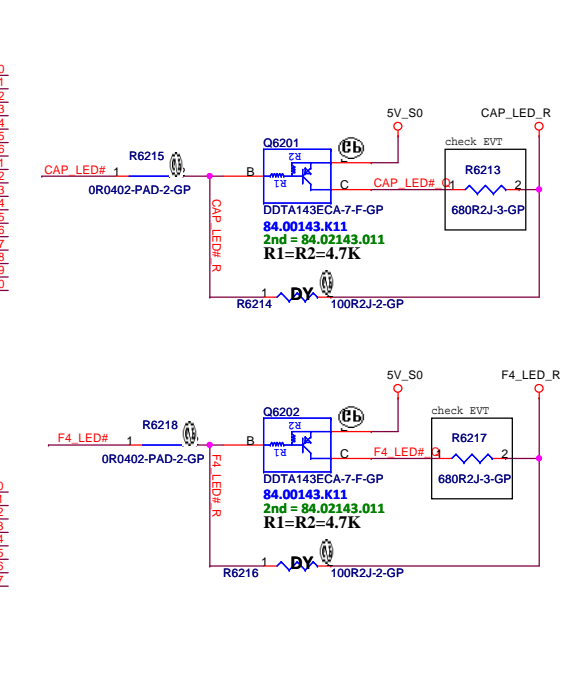
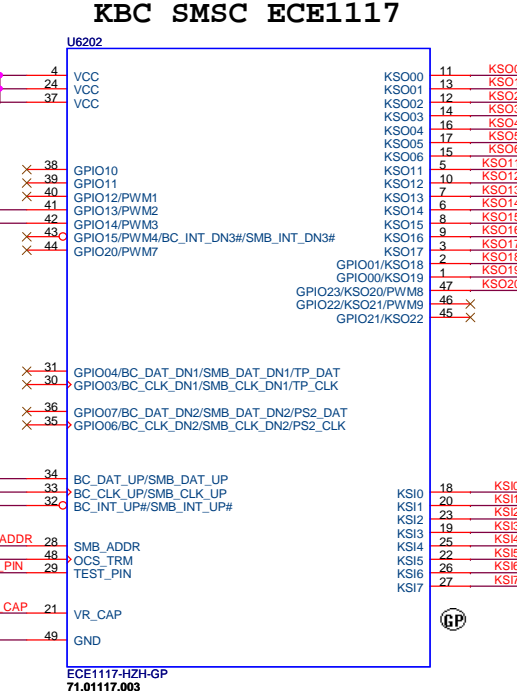
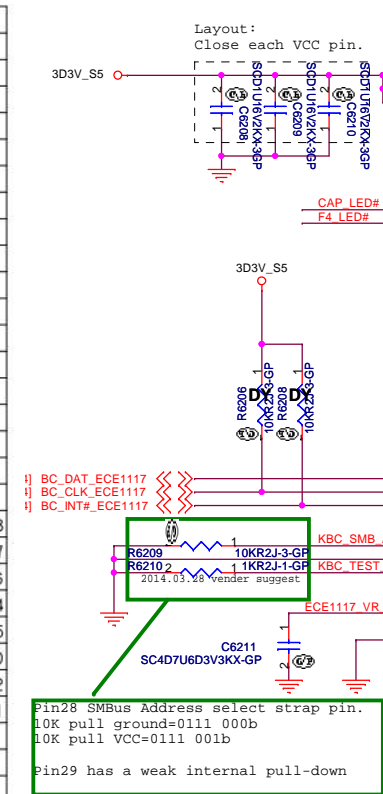


# SSID = KBC

## Internal KeyBoard Connec



PIN#	SIGNAL
1	Diagnostic(LOOP to Pin 31)
2	KS1[7] = KBD S8
3	KS1[6] = KBD S7
4	KS1[4] = KBD S5
5	KS1[2] = KBD S3
6	KS1[5] = KBD S6
7	KS1[1] = KBD S2
8	KS1[3] = KBD S4
9	KS1[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[11] = KBD D8
13	KSO[6] = KBD D7
14	KSO[12] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[16] = KBD D13
20	KSO[20] = KBD D17
21	KSO[19] = KBD D16
22	KSO[17] = KBD D14
23	KSO[18] = KBD D15
24	KSO[13] = KBD D10
25	KSO[15] = KBD D12
26	KSO[14] = KBD D11
27	NC
28	NC
29	GND
30	CapsLK_LED
31	GND
32	F4_LED



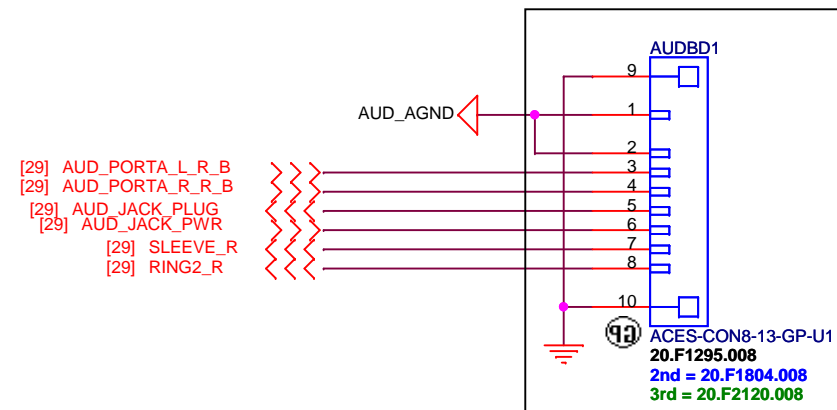
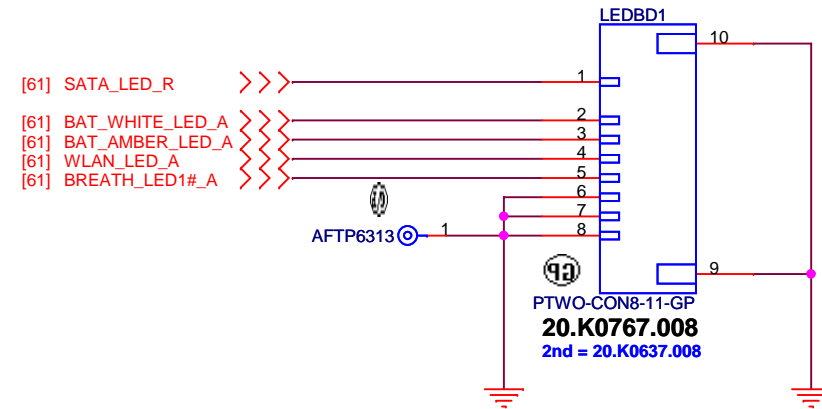
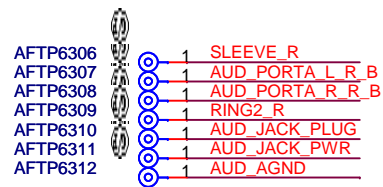
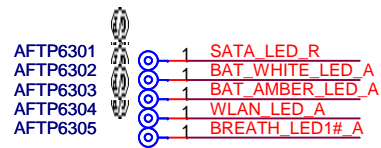
<Core Design>

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Title: **Key Board/Touch Pad**

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2014.06.03 Modify pin assign for connector change

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Title

**IO CONN**

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Title <b>Hall Sensor</b>			
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SSID = DEBUG PORT

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*Debug connector*

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Title

SENSOR

Size  
A3

Document Number

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Rev

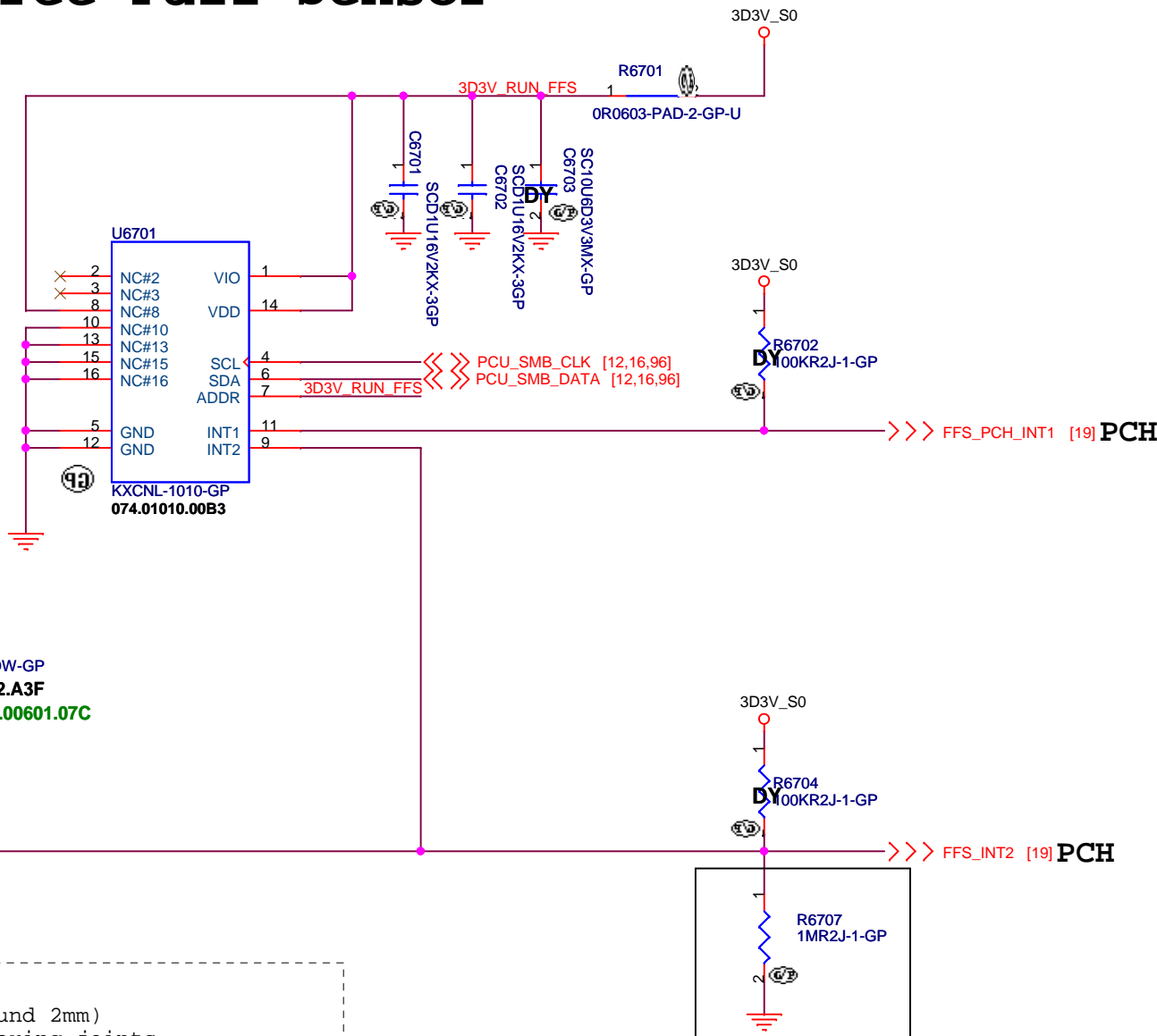
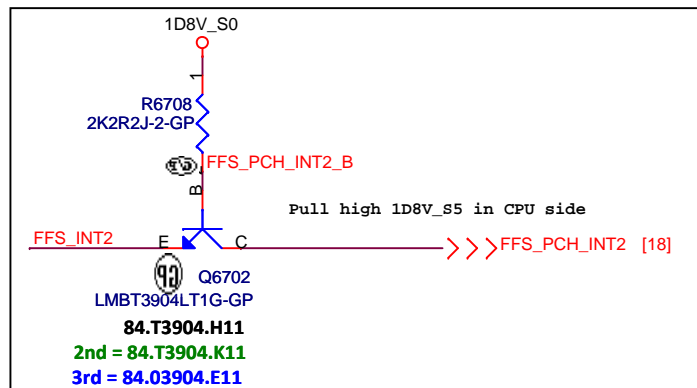
A00

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SSID = User.interface

# Free Fall Sensor

For Kionix FFS as SW proposal 5/15



## Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

## Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

2014.04.24 Venner suggest, reserve to prevent error trigger  
2014.08.28 Change R6707 to 63.10534.1DL for common part

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**Free Fall Sensor**

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**Thunderbolt (1/5)**

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<b><i>Thunderbolt (2/5)</i></b>			
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Title			
<b>Thunderbolt (3/5)</b>			
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Title			
<b>Thunderbolt (4/5)</b>			
Size	Document Number		Rev
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Title			
<b>Thunderbolt (5/5)</b>			
Size	Document Number		Rev
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU (1/5) PEG</b>			
Size	Document Number		Rev
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Title			
<b><i>GPU (2/5) DIGITAL</i></b>			
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Title			
<b>GPU (3/5) VRAM</b>			
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Title			
<b>GPU (4/5) GPIO</b>			
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Title			
<b>GPU (5/5) PWR/GND</b>			
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Title <b>VRAM1,2 (1/4)</b>			
Size A	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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Title <b>VRAM3,4 (2/4)</b>			
Size A	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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Title			
<b>VRAM5,6 (3/4)</b>			
Size	Document Number		Rev
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<b>VRAM7,8 (4/4)</b>			
Size	Document Number		Rev
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( Blanking )

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Title			
<b>VGA CORE</b>			
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Title			
<b>DISCRETE VGAPOWER</b>			
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Title

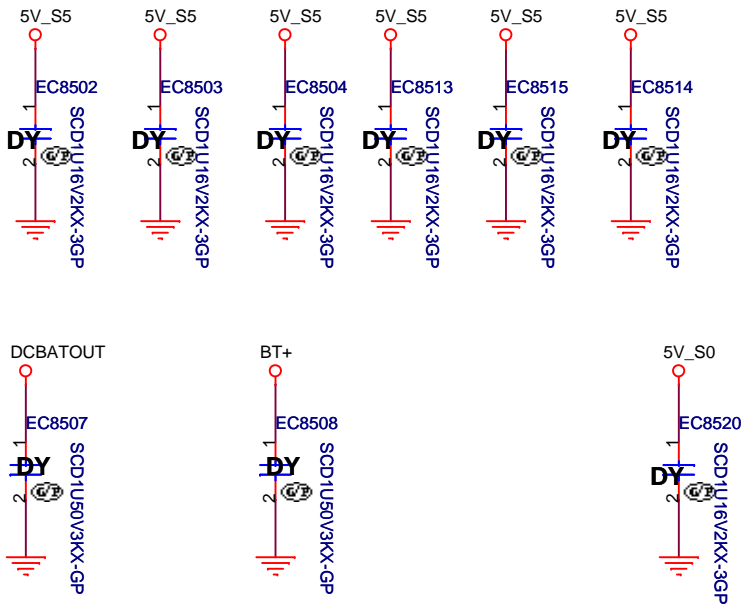
**Switchable GFXLCD**

Size  
A

Document Number  
**Plano 11.6" BTM**

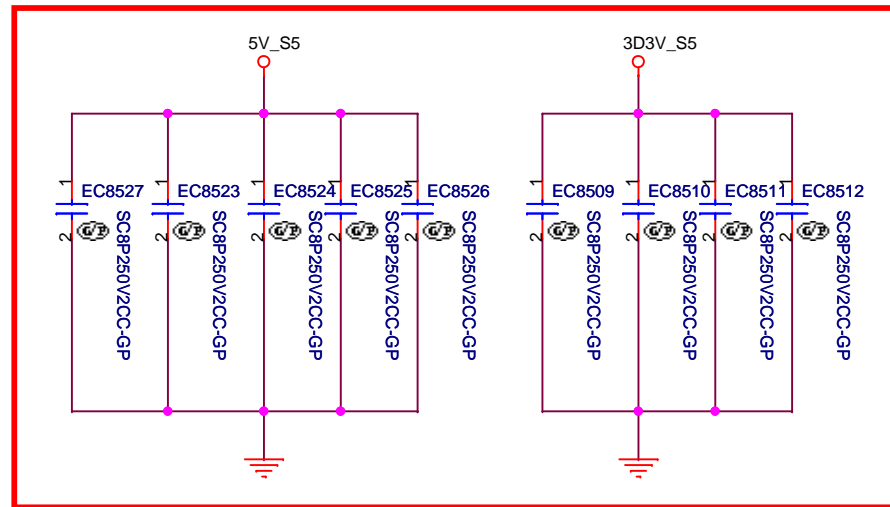
Rev  
**A00**

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2014.09.03 DVT1 EMC add

10/24/2014 DVT2 add for RF cap

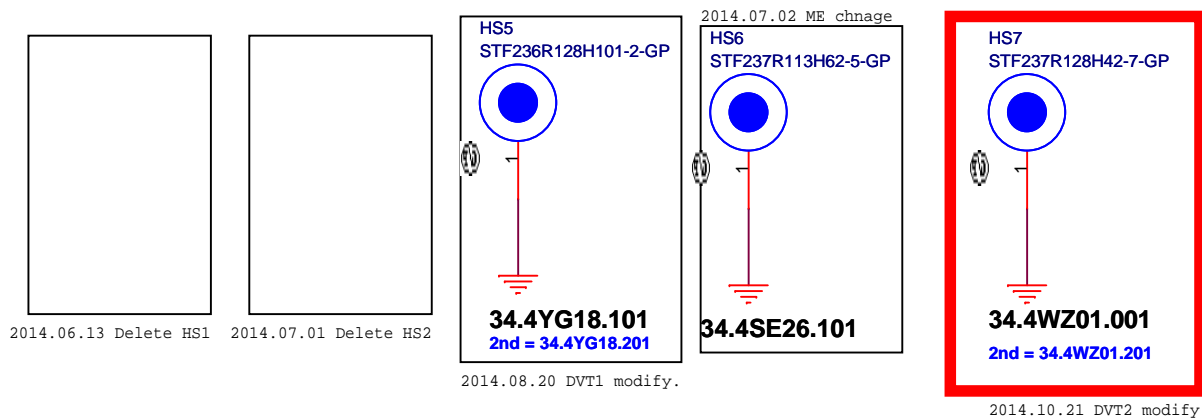
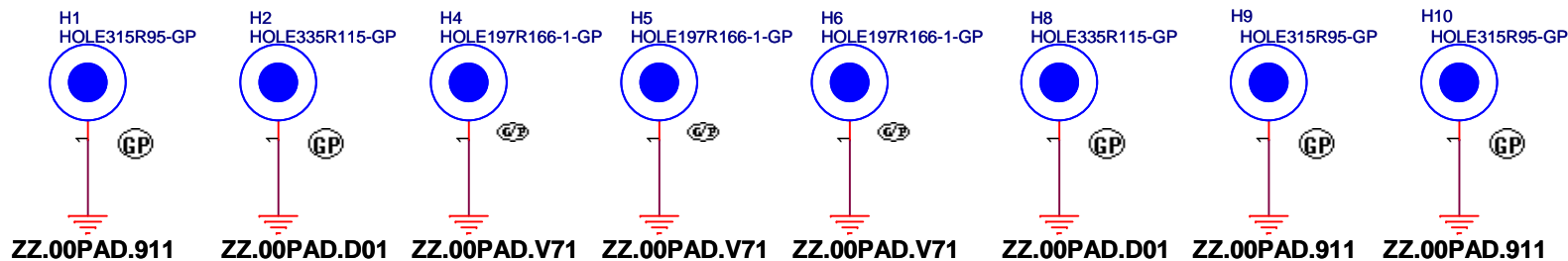
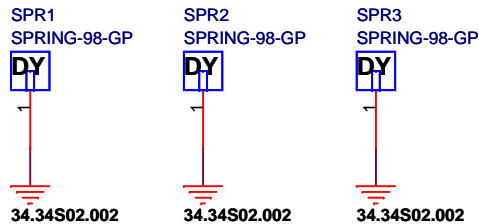


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Title <b>UNUSED PARTS/EMI Capacitors</b>		
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<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>UNUSED PARTS/EMI Capacitors</b>			
Size	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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SSID = USH

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Taipei Hsien 221, Taiwan, R.O.C.

Title

***USH Board Connector***

Size  
A4

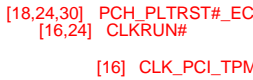
Document Number  
**Plano 11.6" BTM**


Rev  
**A00**

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**SSID = TPM**



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***TPM***

Size

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<Core Design>

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Title <b>USB 2.0 Hub</b>			
Size A4	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>USB 3.0 Controller</b>			
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			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Smart Card</b>					
Size	Document Number <b>Plano 11.6" BTM</b>				Rev <b>A00</b>
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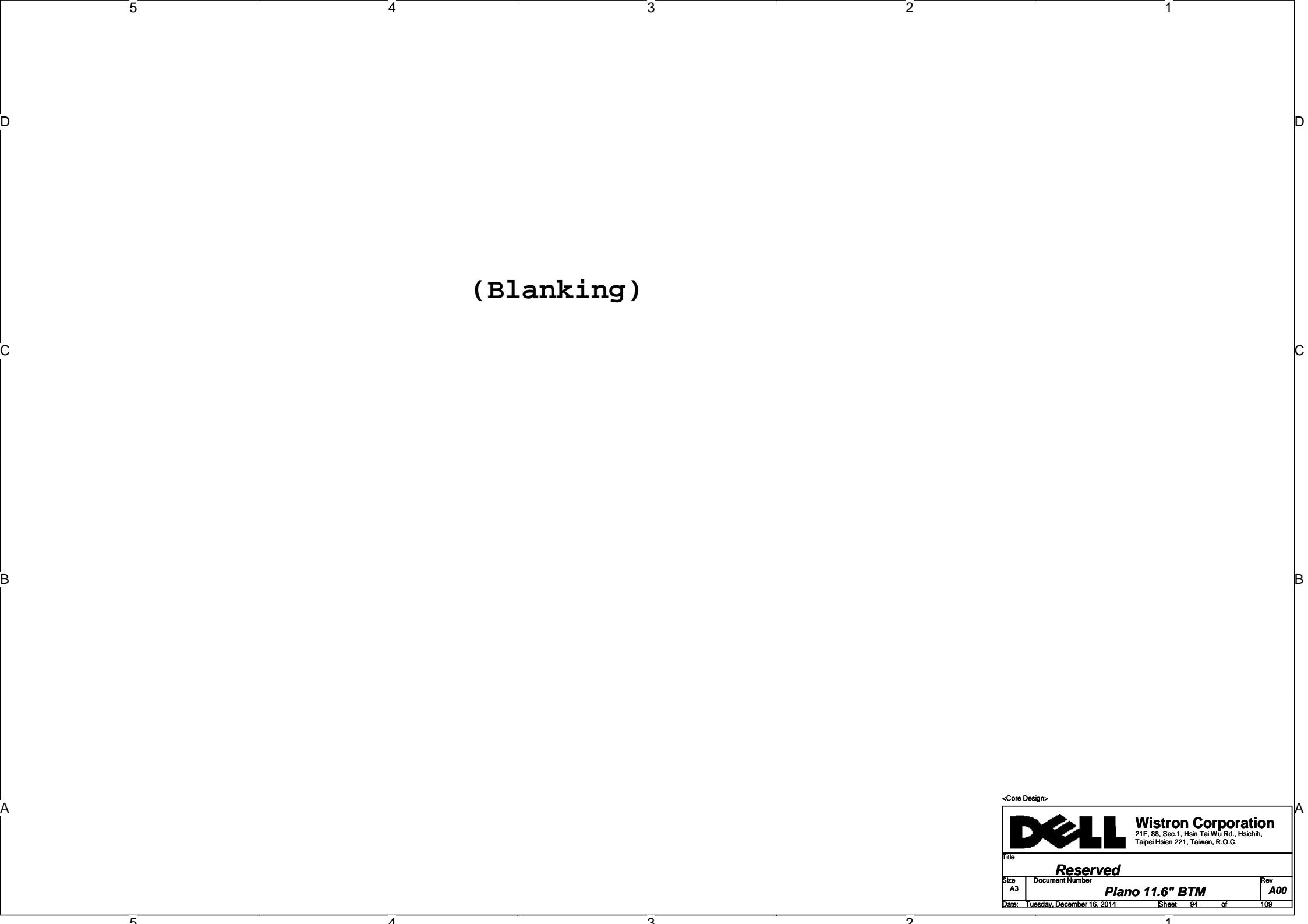
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Title <b>Reserved</b>			
Size A	Document Number <b>Plano 11.6" BTM</b>		Rev <b>A00</b>
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SSID = Docking

( Blanking )


<Core Design>

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Title <b>DOCKING</b>			
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Title

**Reserved**

Size	Document Number	Rev
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5

4

3

2

1

D

D

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B


B

A

A

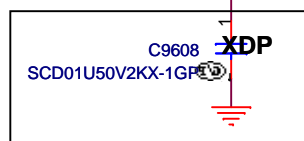
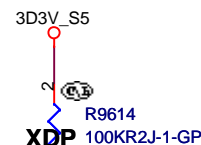
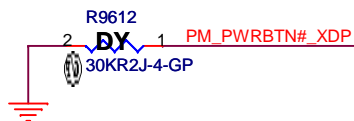
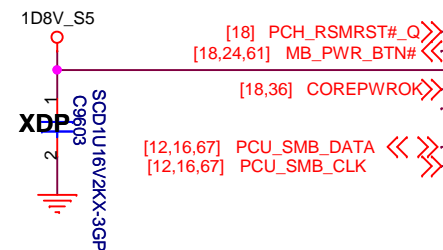
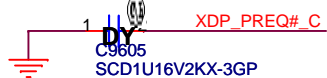
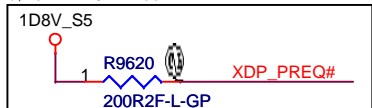
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# SSID = CPU\_XDP

6/19 BTM CRB:200Ω



2014.06.23 Add for sequence

2N7002KDW-GP  
84.2N702.A3F  
2nd = 75.00601.07C

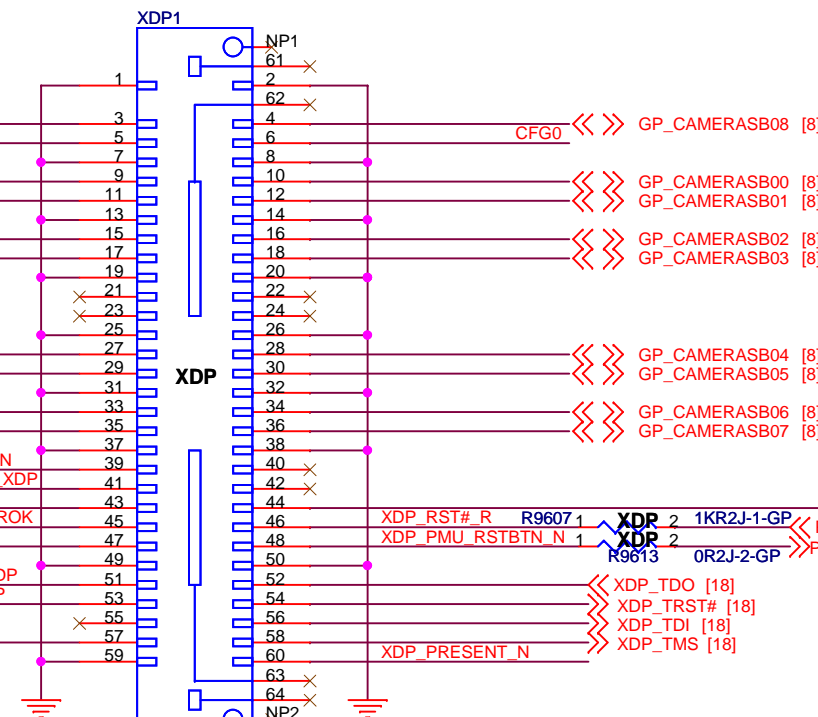
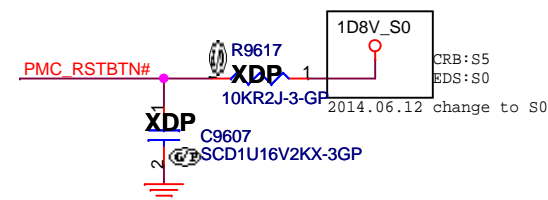
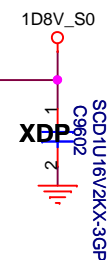
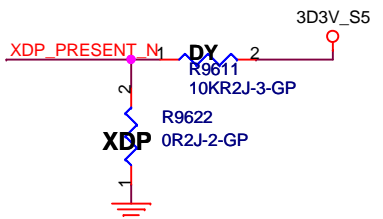
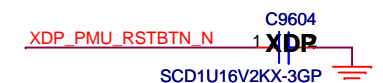
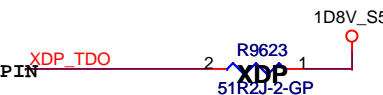
A00 ZZ.00PAD.Q81

## CPU\_XDP

(CRB#509728)

Layout Note:

PLACE R9623 WITHIN 0.25" FROM XDP PIN



A00 ZZ.00PAD.Q81

<Core Design>



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Title		
CPU XDP		
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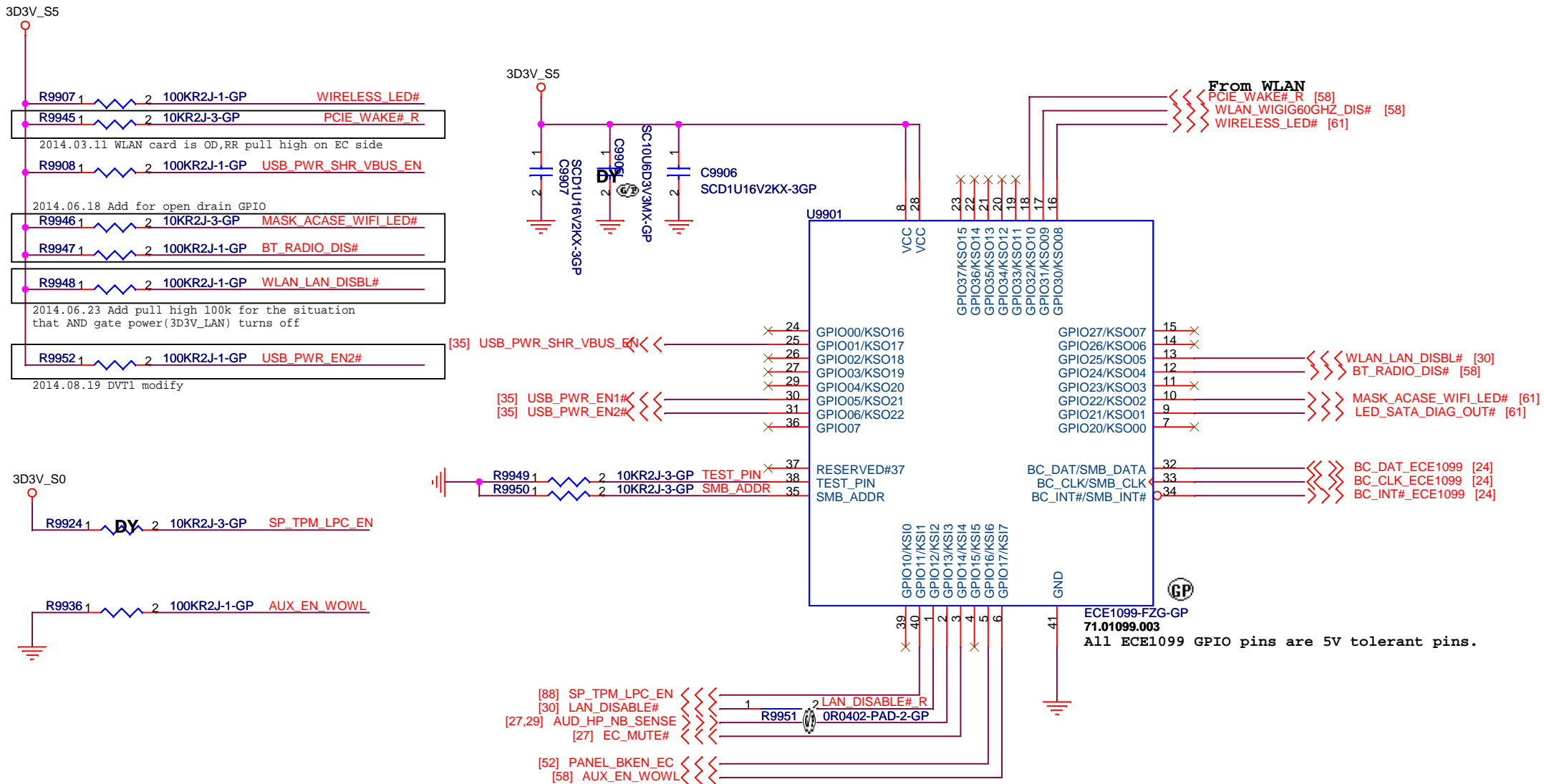
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Title					
<b>USB2.0 HUB</b>					
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# SSID = SIO



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Title

**SIO - ECE1099**

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A4

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### USB2.0 MCP Side

Pair	Device
0	USB port 1 (usb charger)
1	USB port 2
2	WLAN (BT)
3	CAMERA

### USH Side

Pair	Device
0	NA
1	NA

### USB HUB Side

Pair	Device
1	NA
2	NA
3	NA
4	NA

### USB3.0 MCP Side

Pair	Device
1	USB port 1
2	N/A
3	N/A
4	N/A

### PCIE Table

PCIE	
Lane	Device
1	NA
2	Card Reader
3	WLAN
4	LOM

### SATA Table

SATA	
Pair	Device
0	HDD
1	NGFF SSD

## Processor Strapping

Table 20. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is inverted 1 = Top address bit is unchanged
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDIO_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDIO Detect 0 = DDIO not detected 1 = DDIO detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

Bay trail M Processor Schematic Checklist

<Core Design>



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Title

**Table of Content**

Size  
A4

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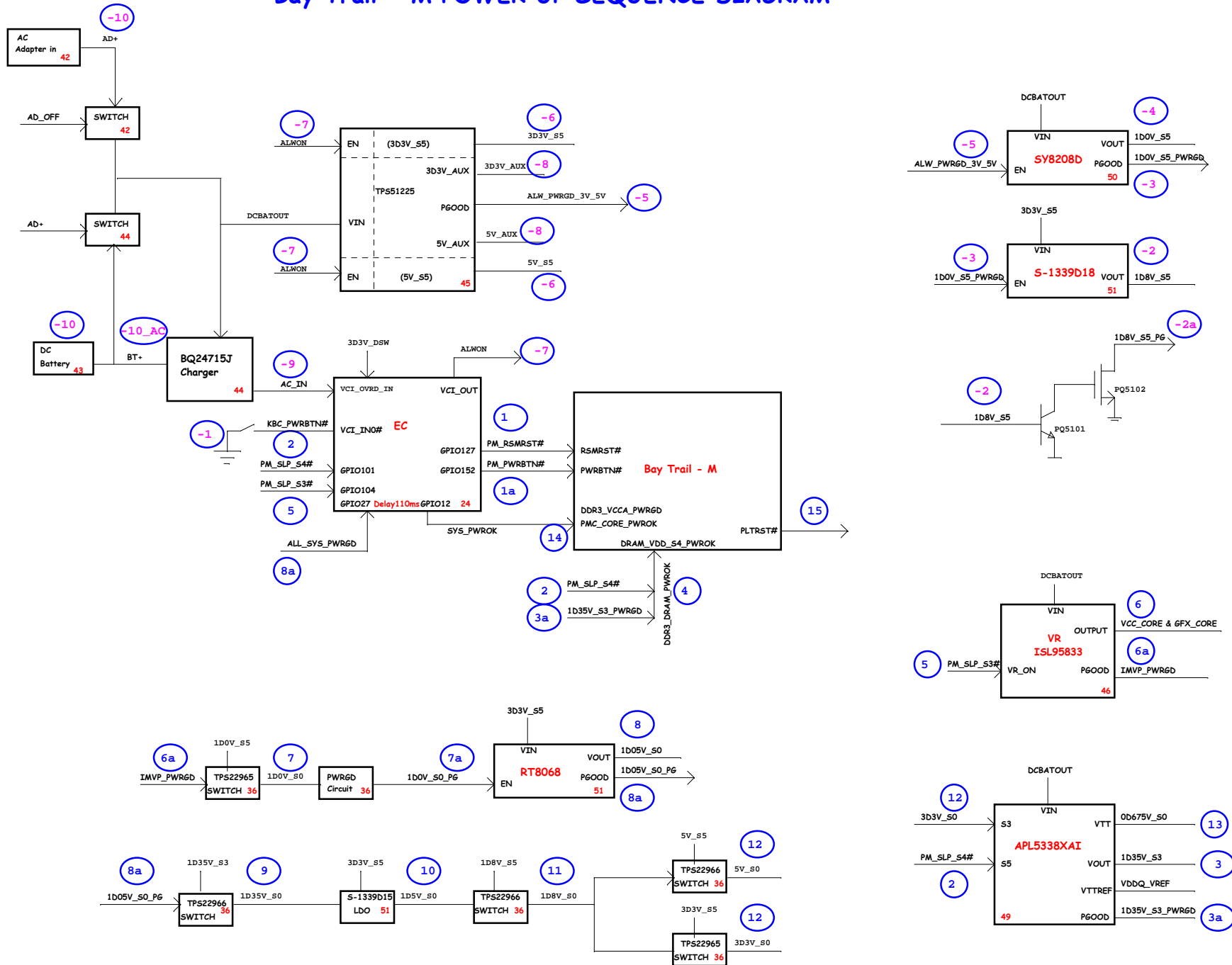
**Plano 11.6" BTM**

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# Bay Trail - M POWER UP SEQUENCE DIAGRAM

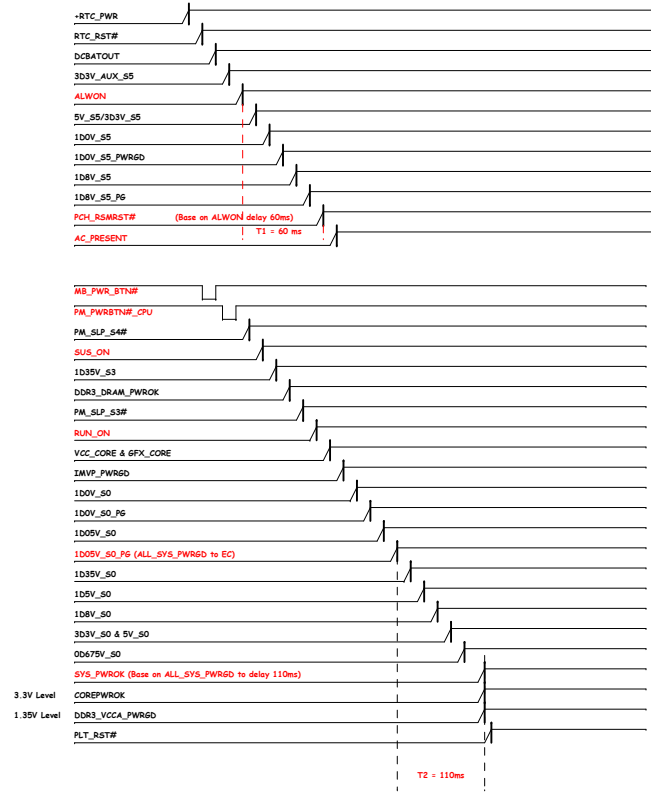


<Core Design>

## Intel-Power Up Sequence with non-S0ix

(AC mode)

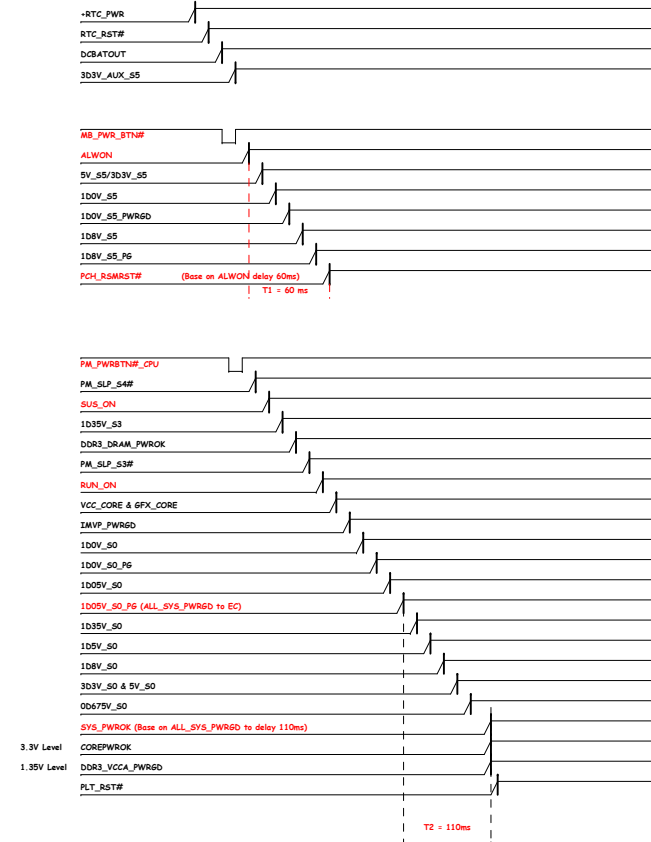
Red word : RBC GPIO



## Intel-Power Up Sequence with non-S0ix

(DC mode)

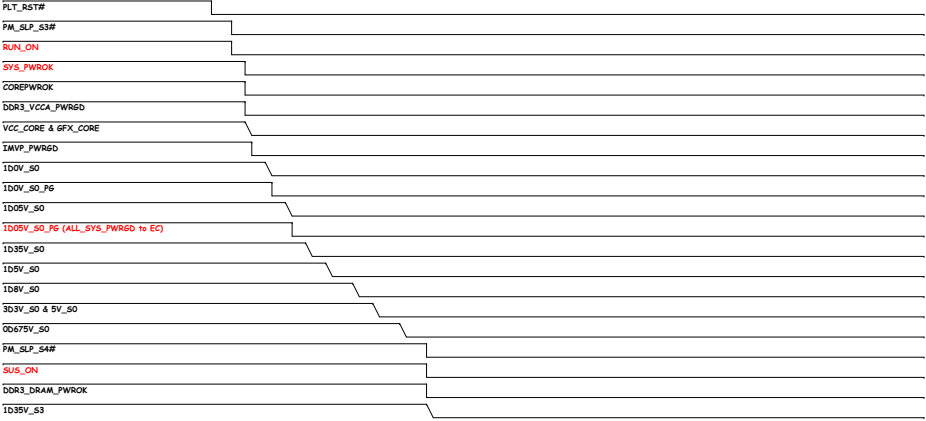
Red word : RBC GPIO



Intel-Power Down Sequence

(AC mode)

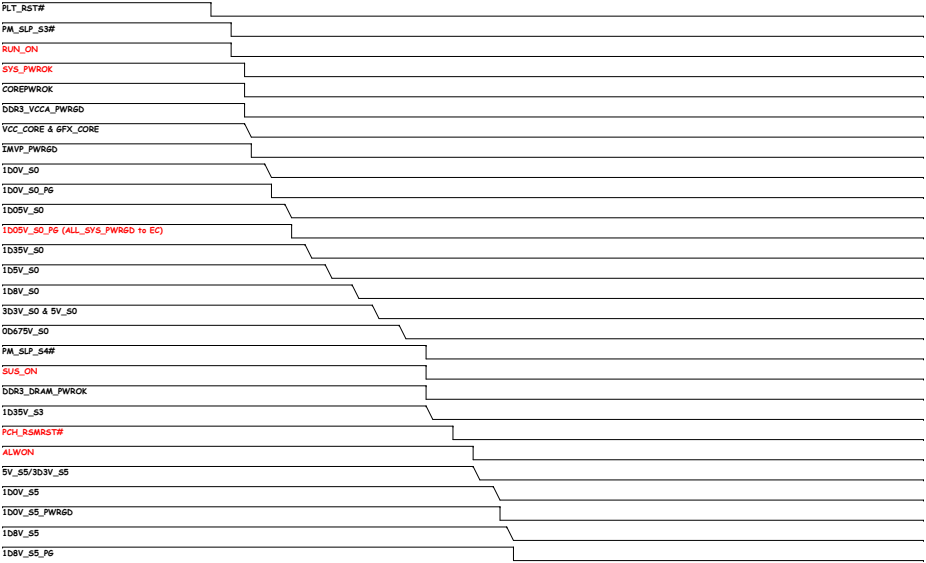
Red word : X8C QP10

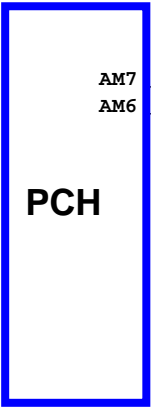


Intel-Power Down Sequence

(DC mode)

Red word : X8C QP10





AM7  
AM6

SMB\_DATA  
SMB\_CLK

2.2K

2.2K

1D8V\_S0

DMN5L06K  
DMN5L06K

2.2K

2.2K

3D3V\_S0

PCU\_SMB\_DATA  
PCU\_SMB\_CLK

200  
202



SMB Addr=[A0]

SML0\_DATA\_XDP  
SML0\_CLK\_XDP

51  
53



SMB Addr=[XX]

6  
4



SMB Addr=[3A]

**TCA9406**

Bus  
Bus

ADDR pin status	SAD	SAD + Read	SAD + Write
ADDR = 0	0011110 (1Eh)	00111101 (3Dh)	00111100 (3Ch)
ADDR = 1	0011101 (1Dh)	00111011 (3Bh)	00111010 (3Ah)

Bus Specification V1.1, which can be downloaded from [www.smbus.org](http://www.smbus.org). The bq24715/7 uses the SMBus Read-Word and Write-Word protocols (Figure 4) to communicate with the smart battery. The bq24715/7 performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus. In

A5 B6

**EC**

**MEC5085**

A47  
B50

CHARGER\_SMBDAT  
CHARGER\_SMBCLK

2.2K

2.2K

3D3V\_S5

8  
9



SMB Addr=[12]

2.2K

2.2K

3D3V\_S5

PBAT\_SMBDAT  
PBAT\_SMBCLK

PBAT\_SMBDAT\_R  
PBAT\_SMBCLK\_R

4  
3

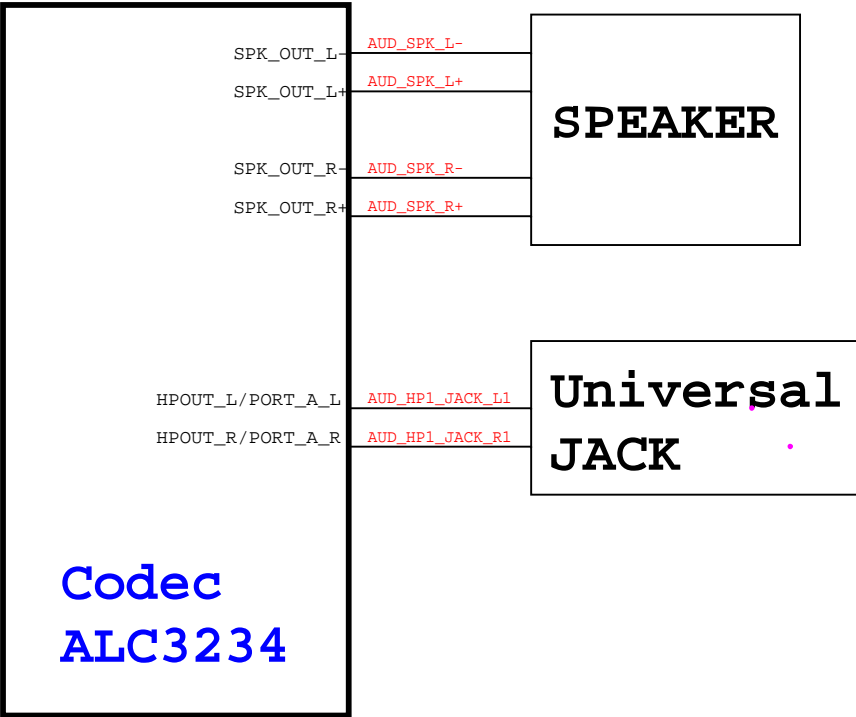
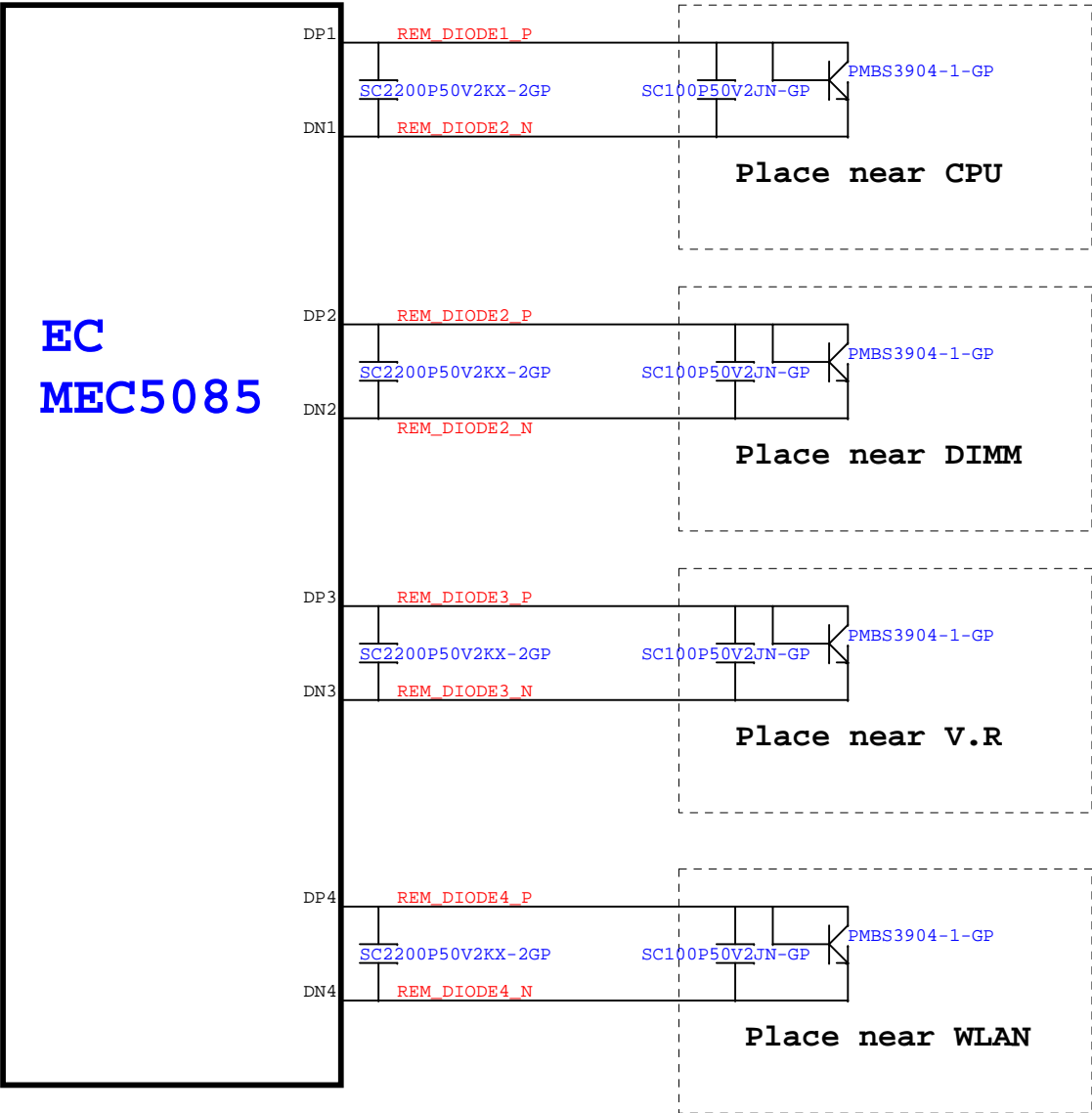


SMB Addr=[16]




# Thermal Block Diagram

# Audio Block Diagram



<Core Design>

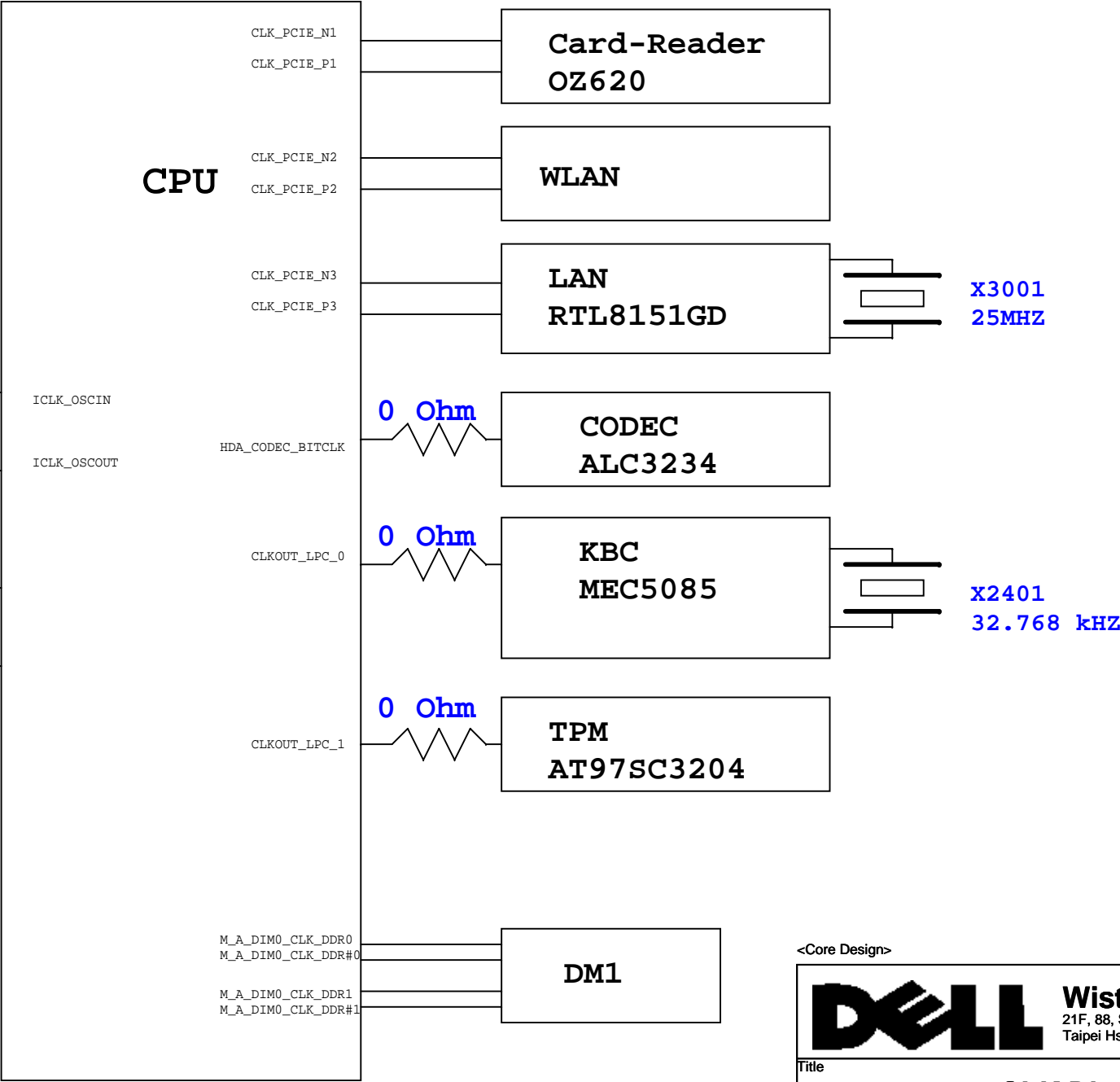
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Title <b>Thermal/Audio Block Diagram</b>			
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<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>CLK Block</b>					
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